
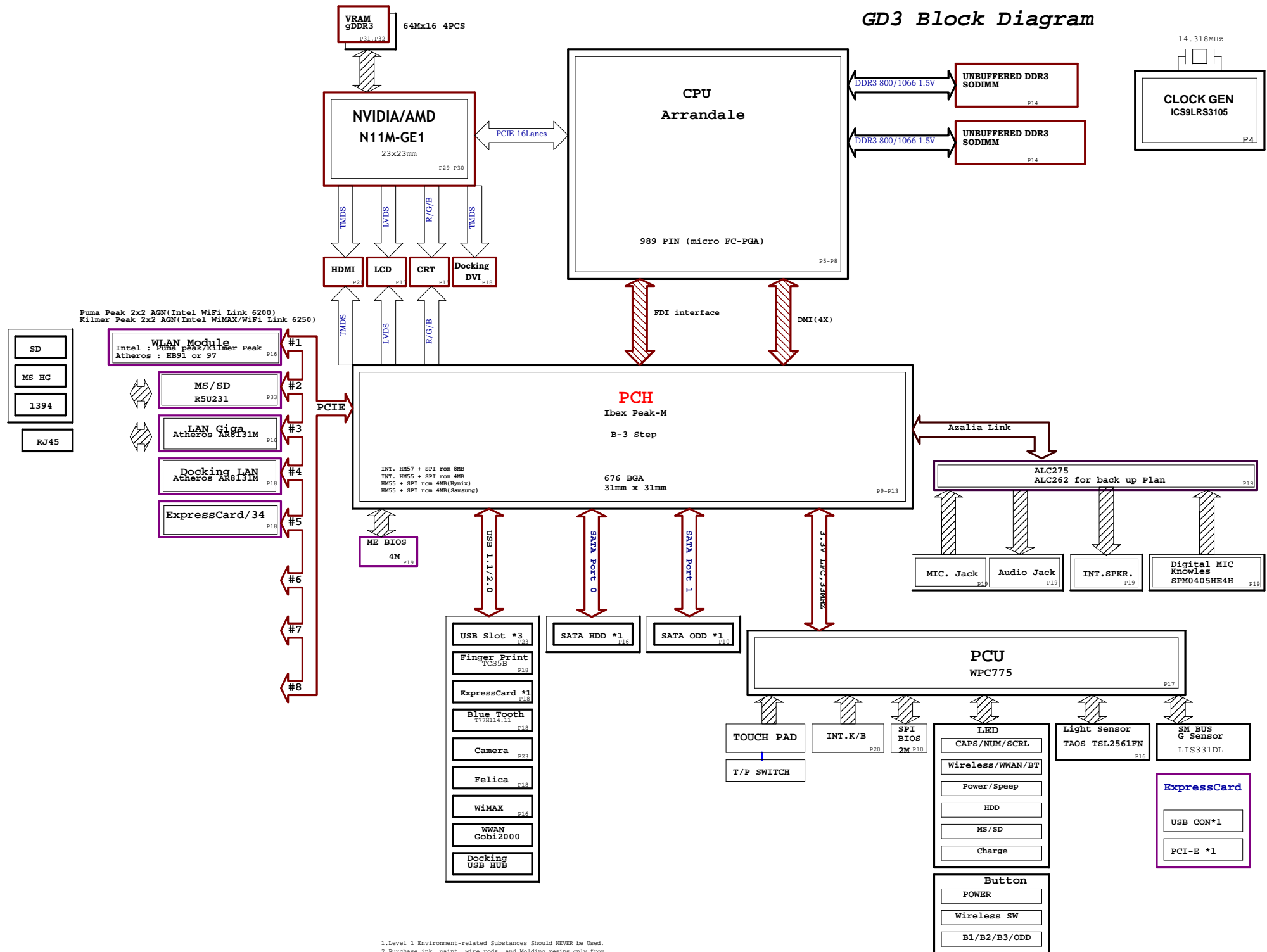


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03	Change List	1A	
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06	PROCESSOR 2/4(DDR)	1A	
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08	PROCESSOR 4/4(GND)	1A	
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18	Docking/35001/TP/S1	1A	
19	HDD/ODD/SSD	1A	
20	KB/USB/FAN/Reset	1A	
21	HDMI	1A	
22	POWER CPU CORE (ISL62882)	1A	
23	POWER 3VPCU&5VPCU(PM6686)	1A	
24	POWER 1.5VSUS/VTT_MEM	1A	
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29	NVIDIA N11M-GE1 PCIE&PW 1/3	1A	
30	NVIDIA N11M-GE1 TMDS&DAC 2/3	1A	
31	NVIDIA N11M-GE1 VRAM 3/4	1A	
32	NVIDIA N11M-GE1 VRAM 4/4	1A	
33	R5U231	1A	

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GD3 Block Diagram




PVT change list

I010:

- P5 Delete R21 0 ohm.(Cost down)
- P7 C56 mount only in Intel.
- P7 Delete R45,R46(Cost down)
- P10 Delete R132(Cost down)
- P10 Add R636,R637,R638 100K.
- P11 Delete RP11,RP12,RP13,RP14,RP15,RP9,RP10.(Cost Down)
- P12 Delete RP16
- P13 Delete R580.(Cost Down)
- P16 Delete F13
- P17 Add R639 100K in U23.3.
- P17 Add 5VPGD_775 in U23.3.
- P18 R340 change from 10K to 4.7K.(For 35001 signal)
- P18 CON42 change from 16pin to 14 pin.(For TP/B con)
- P18 Delete R331,R332,R333
- P18 Add L30,L31,L32
- P19 R613 change to 10 ohm
- P19 R588 change from 36K to 34.8K/F.(For ODD test)
- P23 PR72 pin1 change to PM_SYS_PWRGD.(For BIOS protect)
- P23 PR75 pin 1 change to 5VPGD_775.(For BIOS protect)
- P23 Add D61(For BIOS Protect)
- P24 Add PU18 LM393.
- P24 Add PC249 0.1UF.
- P24 Add PR325 100K/F
- P24 Add PR326 12K/F
- P24 Delete PU17
- P24 PC212 change from 2200PF to 0.01UF.
- P26 PR202 change value from 47K/F to 270K/F.
- P27 PU15 change footprint
- P28 PR252 change value from 49.9K to 200K.

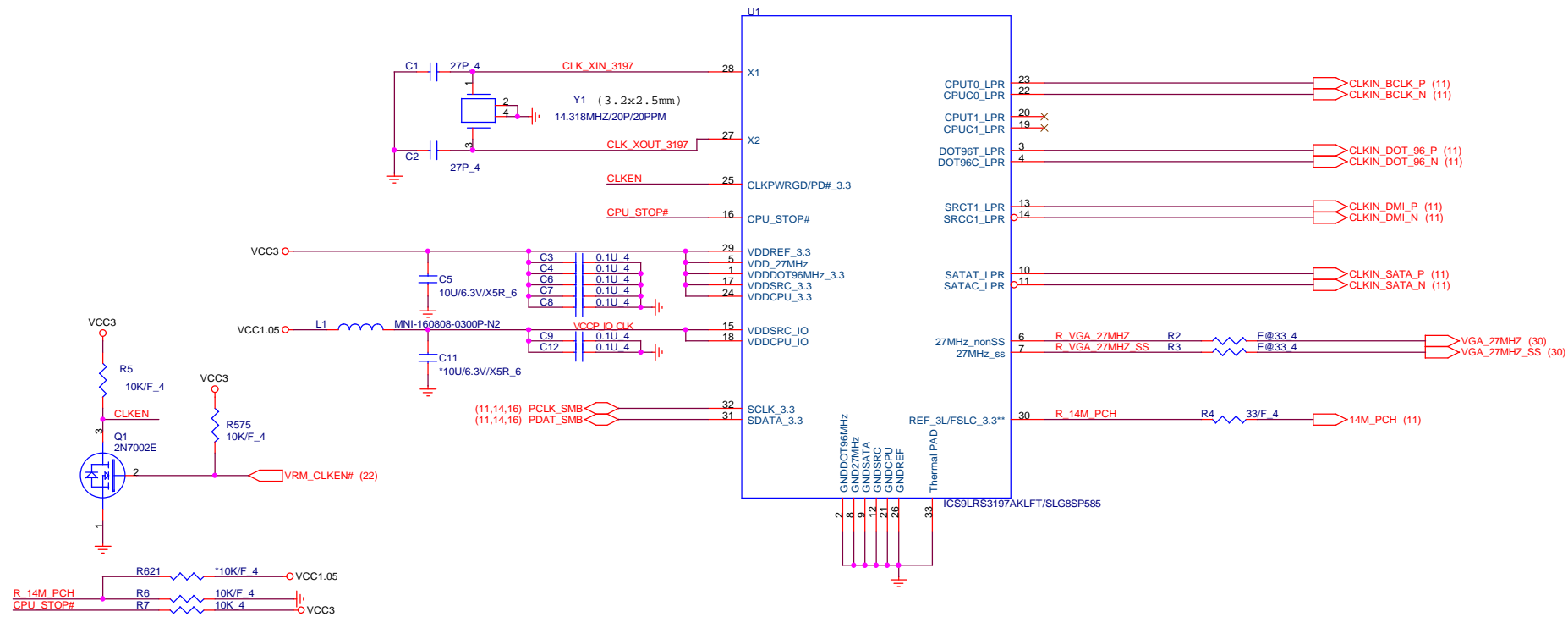
I019:

- P20 Add R640 100K.(For KB BLIGHT initial)



QUANTA
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CPU Frequency Select Table

FSLC	CPU MHz	SRC MHz	REF MHz	USB MHz	DOT MHz
0 (default)	133.33	100.00	14.318	48.00	96.00
1	100.00				

Table 2: pin 6, 7 Configuration

B1b4	B1b3	B1b2	B1b1	Pin 6 MHz	Pin 7 MHz	Spread %	Comment
0	0	0	0	N/A	N/A	N/A	N/A
0	0	0	1	N/A	N/A	N/A	N/A
0	0	1	0	27MHz_nonSS	27MHz_SS	-0.5%	
0	0	1	1	27MHz_nonSS	27MHz_SS	-1%	
0	1	0	0	27MHz_nonSS	27MHz_SS	-1.5%	
0	1	0	1	27MHz_nonSS	27MHz_SS	-2%	
0	1	1	0	27MHz_nonSS	27MHz_SS	-0.75%	
0	1	1	1	27MHz_nonSS	27MHz_SS	-1.25%	
1	0	0	0	27MHz_nonSS	27MHz_SS	-1.75%	
1	0	0	1	27MHz_nonSS	27MHz_SS	+0.5%	
1	0	1	0	27MHz_nonSS	27MHz_SS	+0.75%	
1	0	1	1	N/A	N/A	N/A	N/A
1	1	0	0	N/A	N/A	N/A	N/A
1	1	0	1	N/A	N/A	N/A	N/A
1	1	1	0	N/A	N/A	N/A	N/A
1	1	1	1	N/A	N/A	N/A	N/A

Table 4: Device ID table

B8b7	B8b6	B8b5	B8b4	Comment
0	0	0	0	56 pin TSSOP
0	0	0	1	64 pin TSSOP
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	72 pin QFN
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	32 pin QFN
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Table 3: IO Vout select table

B9b2	B9b1	B9b0	IO_Vout
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V
1	1	0	0.9V
1	1	1	1.0V

**QUANTA
COMPUTER**

Title: **CLOCK GENERATOR**

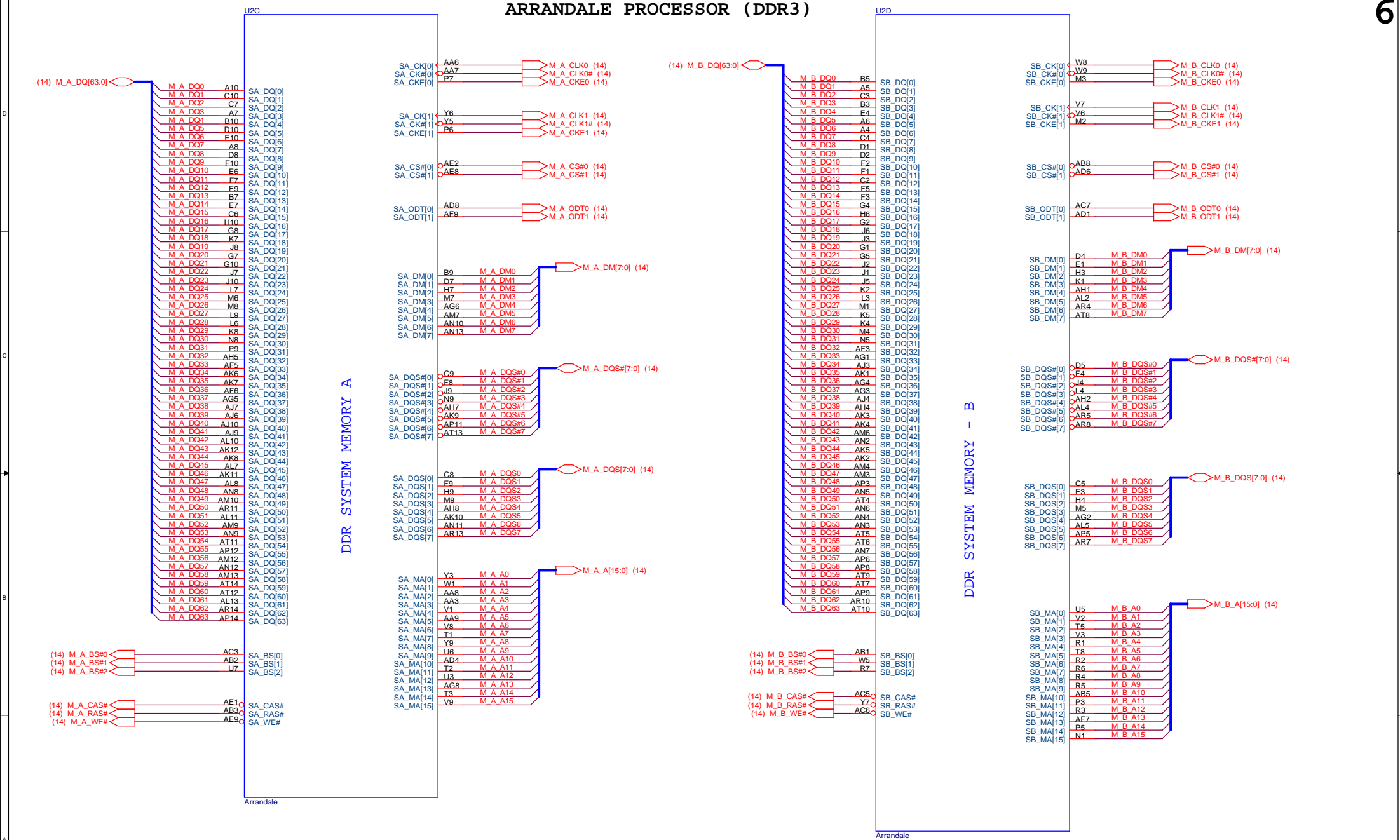
Size: **GD3 Main Board** Rev 1A

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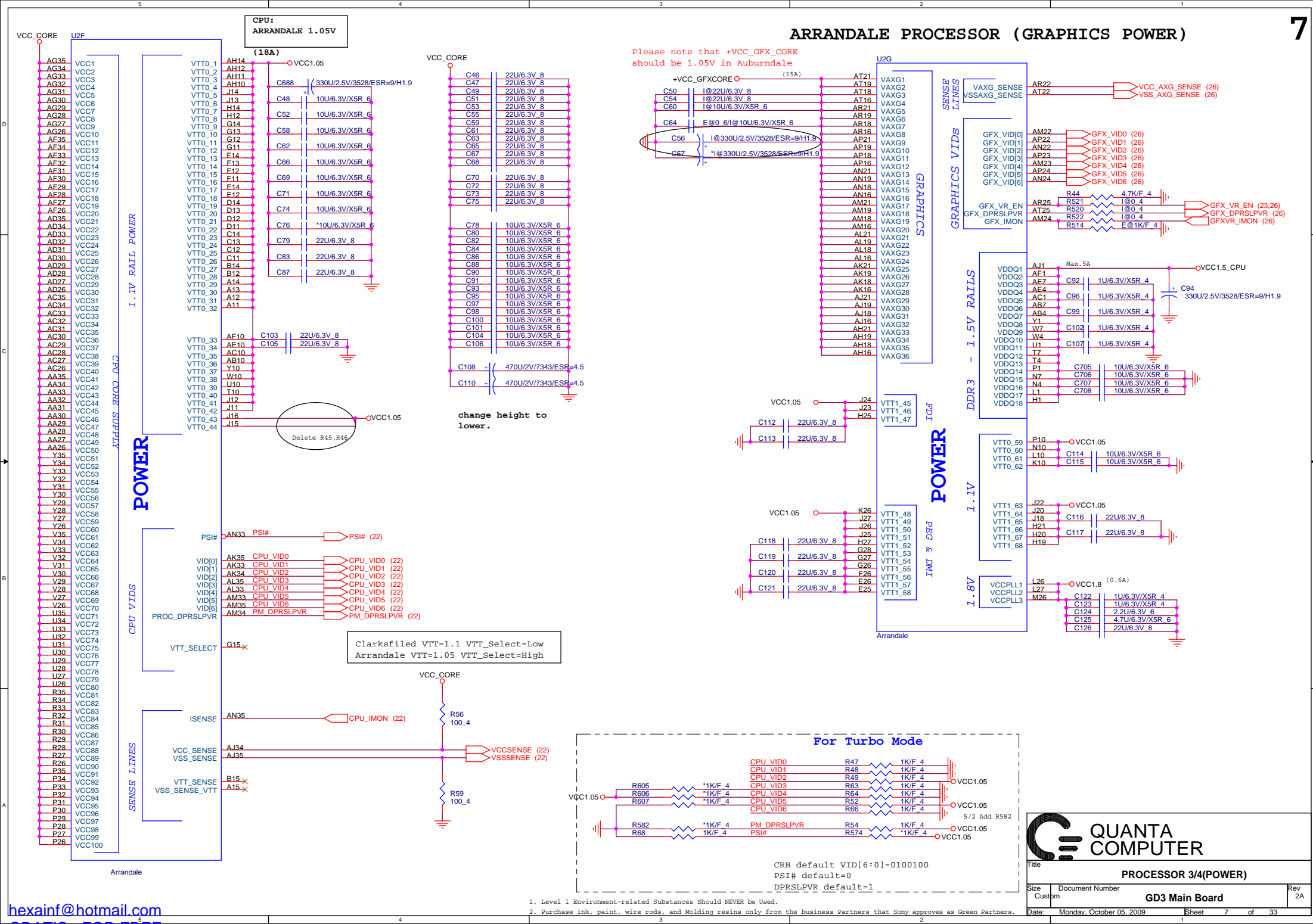
1.Level 1 Environment-related Substances Should NEVER be Used.

2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

ARRANDALE PROCESSOR (DDR3)



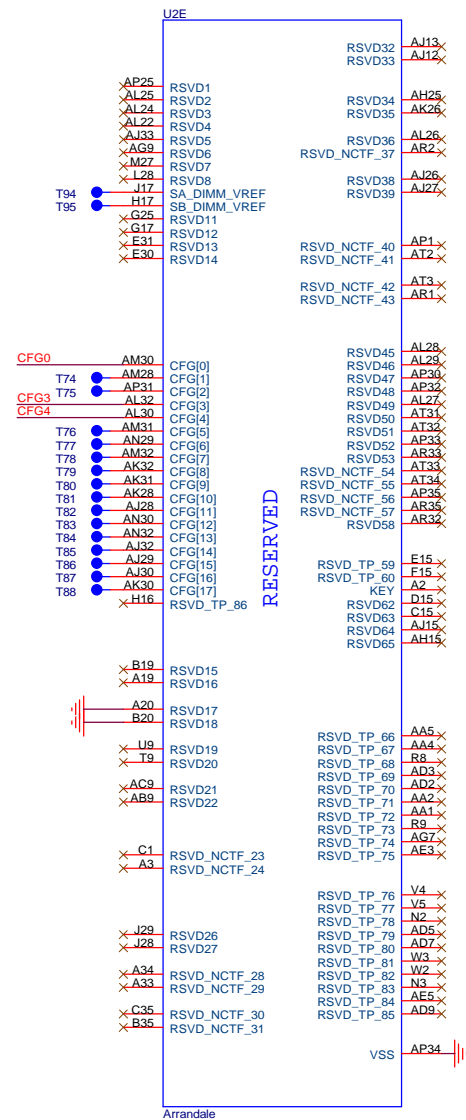
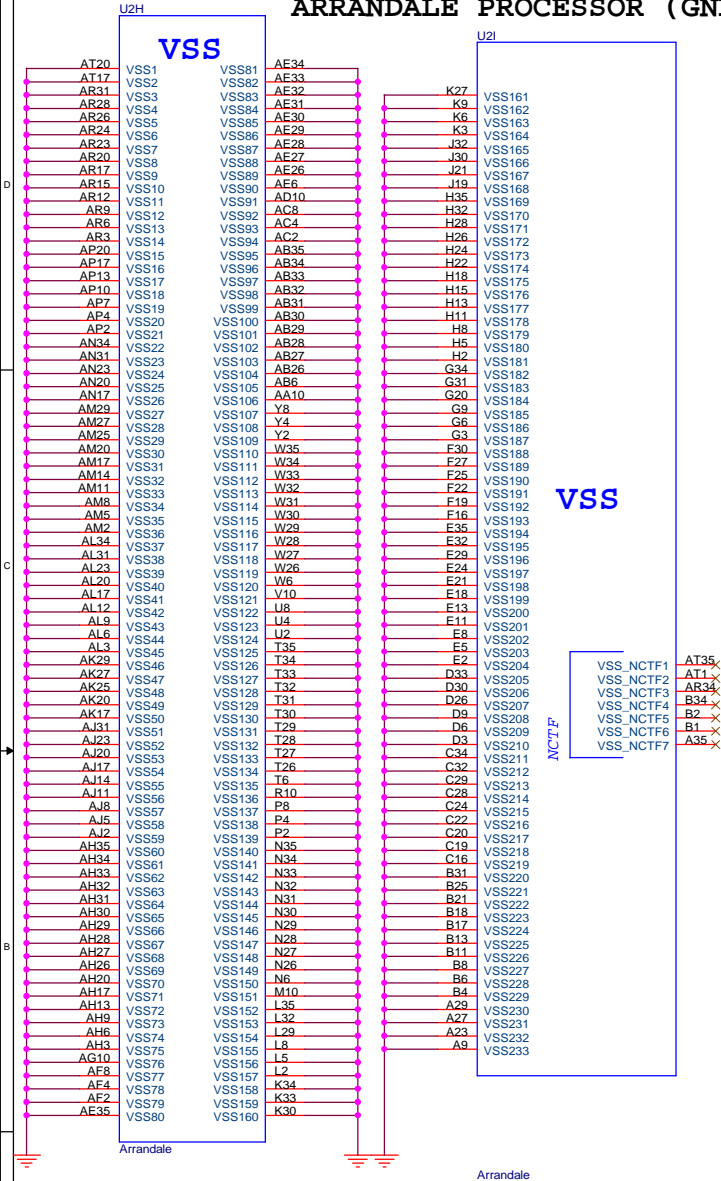
ARRANDALE PROCESSOR (GRAPHICS POWER)



ARRANDALE PROCESSOR (GND)

ARRANDALE PROCESSOR(RESERVED, CFG)

8



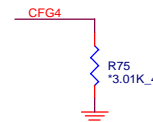
Not applicable for Clarksfield Processor

PCI-Epress Configuration Select	
CFG0	1 : Single PEG 0 : Bifurcation enabled

PCI-Epress Static Lane Reversal	
CFG3	1 : Normal Operation 0 : Lane Number Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display port device is connected to the Embedded Display port
------	--



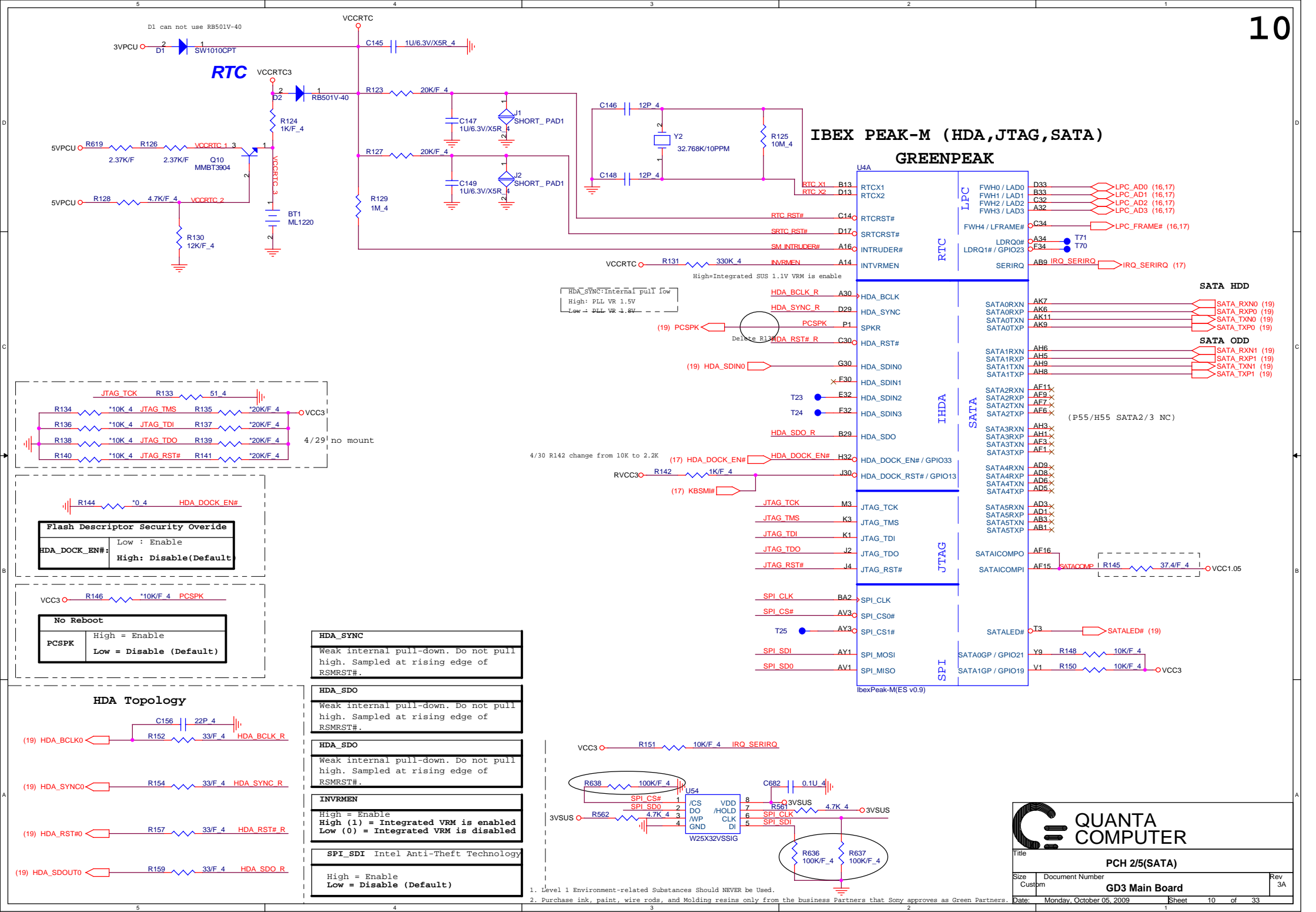
Title				
PROCESSOR 4/4(GND)				
Size	Document Number			Rev
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1. Level 1 Environment-related Substances Should NEVER be Used.

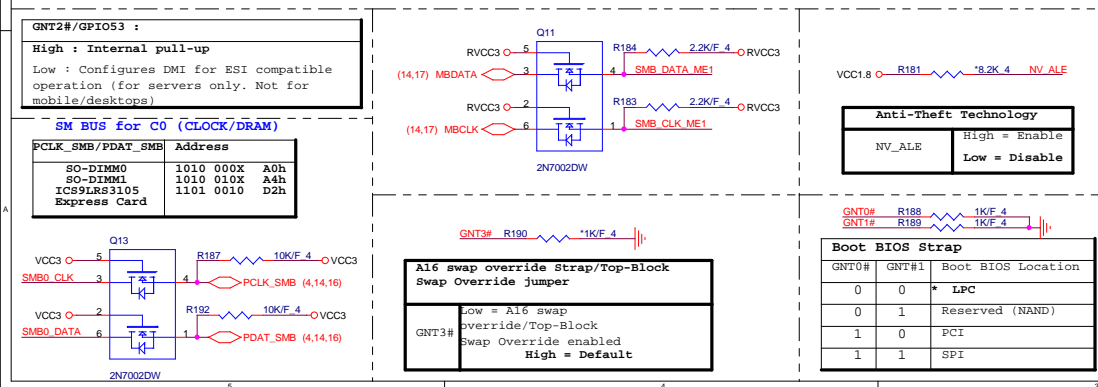
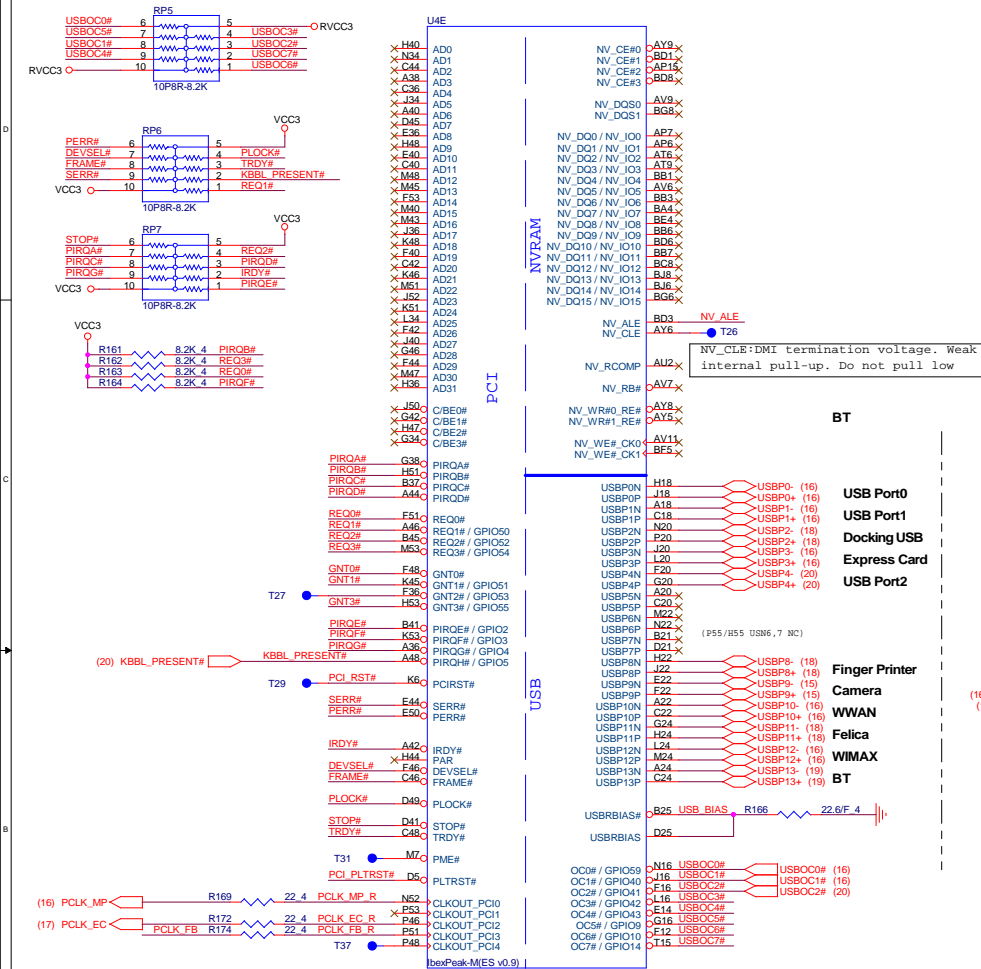
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

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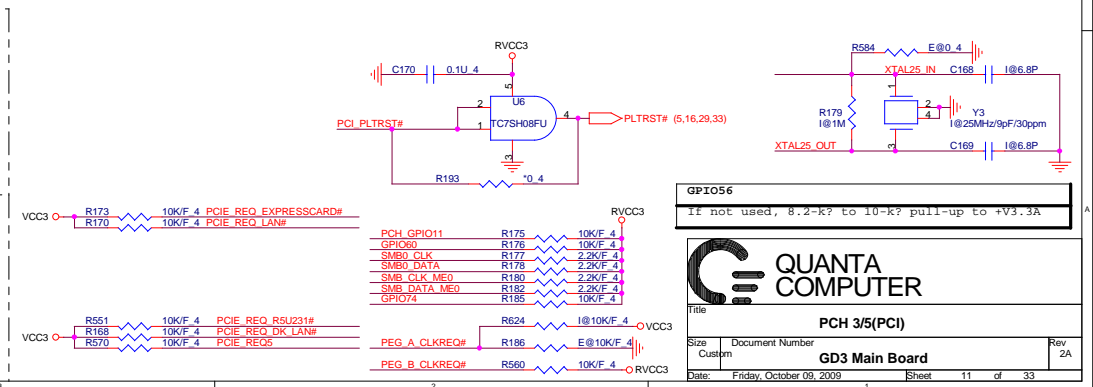
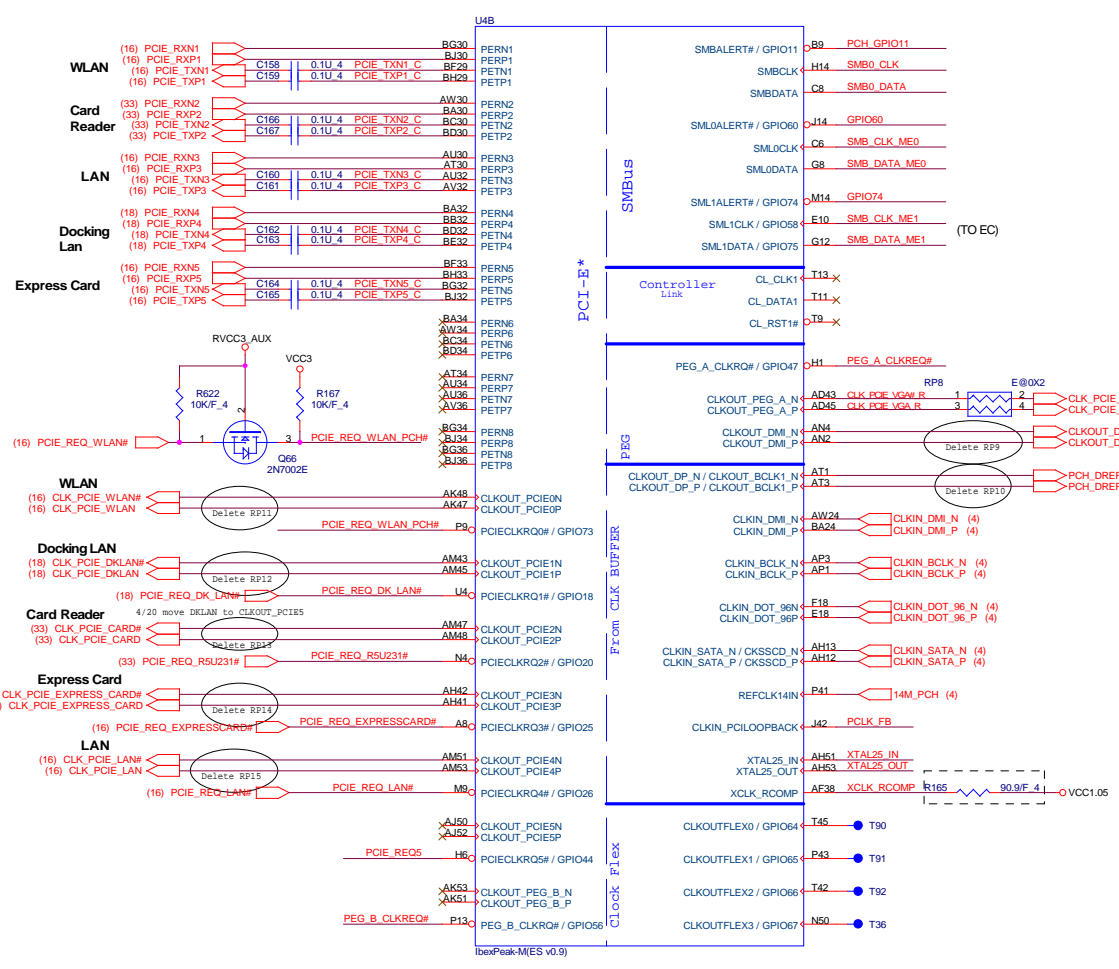




IBEX PEAK-M (PCI,USB,NVRAM)

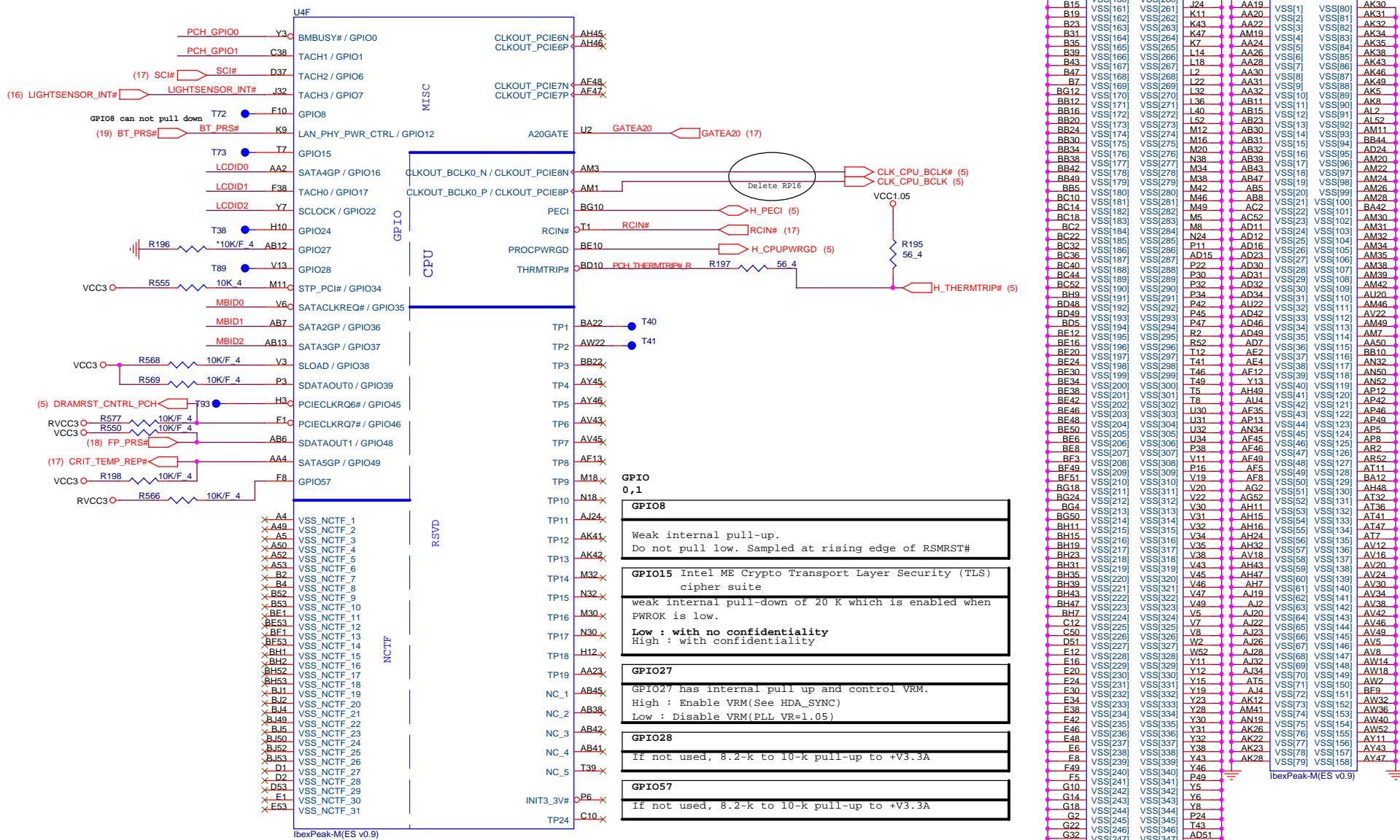


IBEX PEAK-M (PCI-E, SMBUS, CLK)

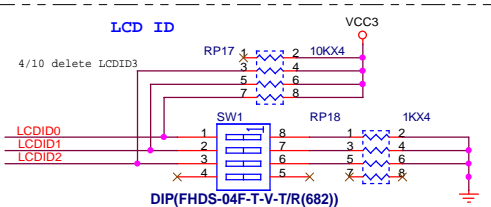


IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

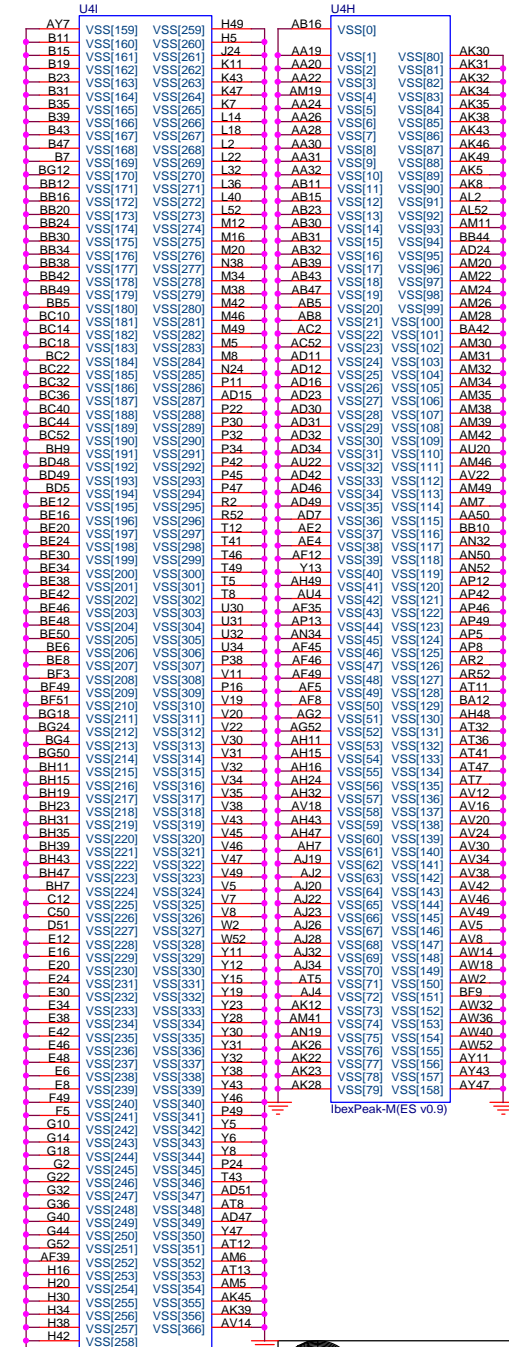
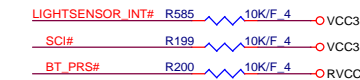
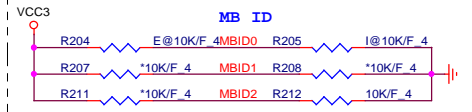
12



SV_SET_UP High = Strong (Default)



	MBID0	MBID1	MBID2	QCI P/N
INT. HM57 + SPI rom 8MB	0	0	0	31GD3MB00030
INT. HM55 + SPI rom 4MB	0	0	1	31GD3MB00000
HM55 + SPI rom 4MB (Hynix)	1	0	0	31GD3MB00010
HM55 + SPI rom 4MB (Samsung)	1	0	1	31GD3MB00020



QUANTA COMPUTER

Title: PCH 4/5(GPIO)

Size: Custom

Document Number: GD3 Main Board

Date: Monday, October 05, 2009

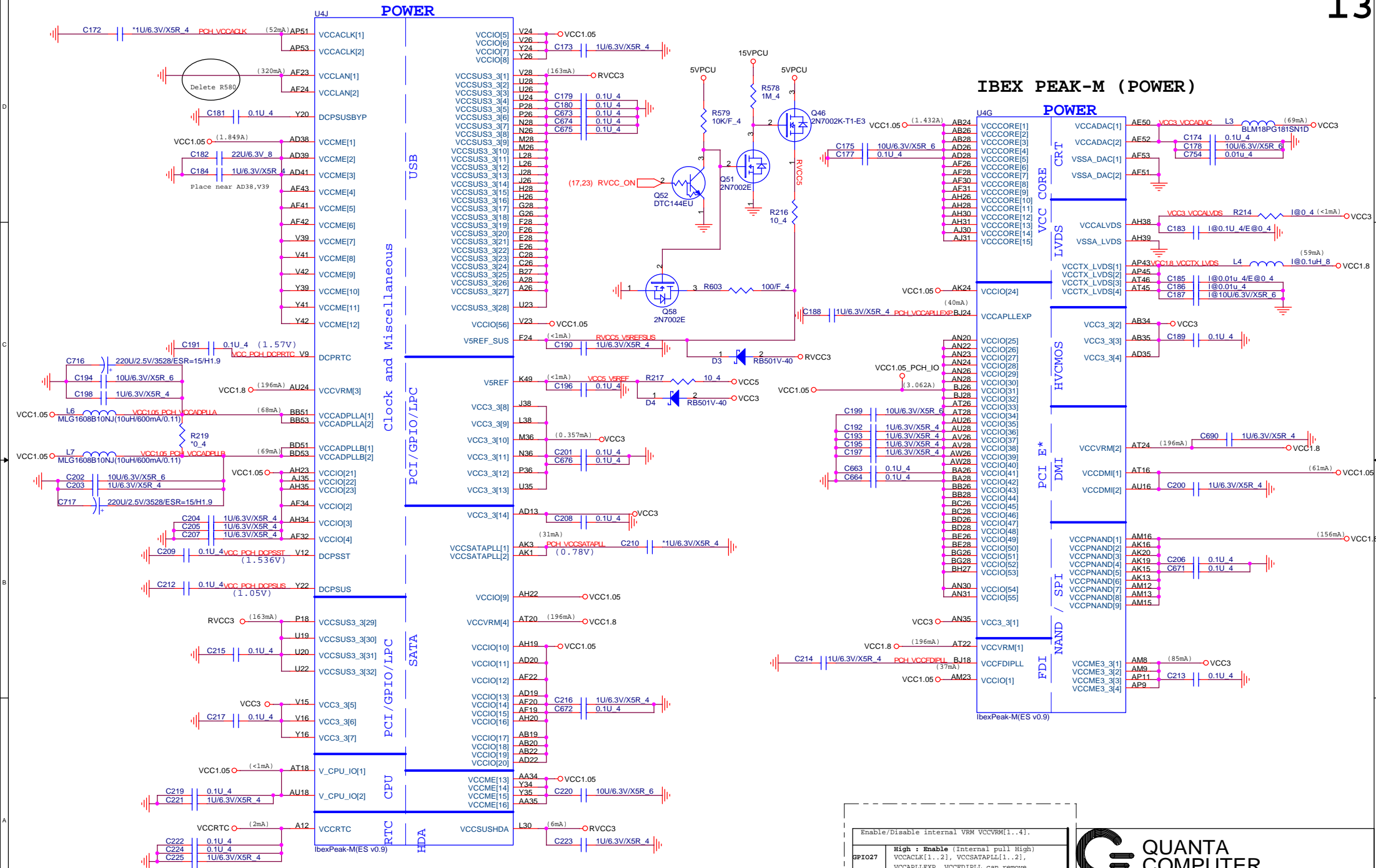
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Rev: 1A

1. Level 1 Environment-related Substances Should NEVER be Used.

2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

IBEX PEAK-M (POWER)



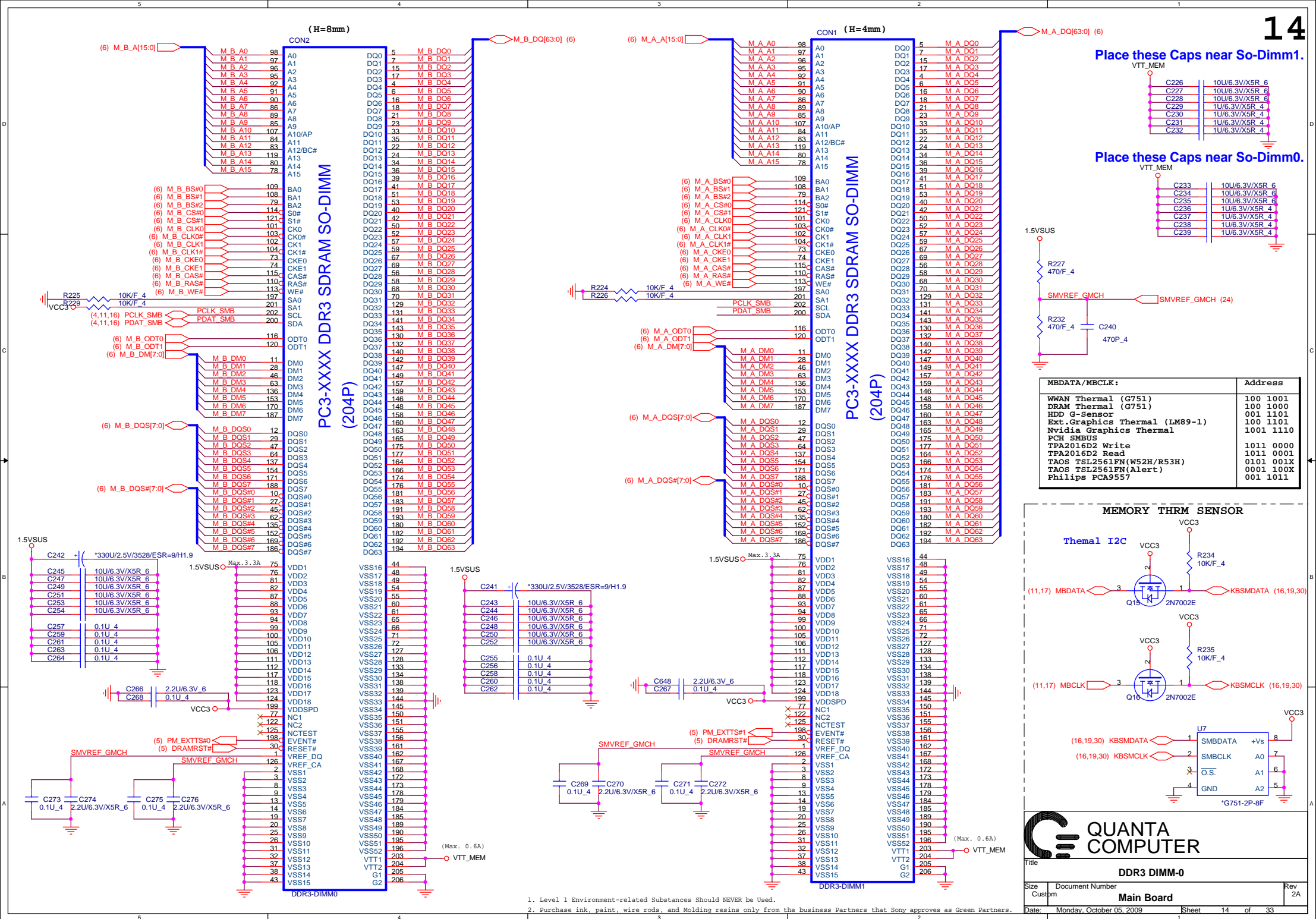
Enable/Disable internal VRM VCCVRM[1..4].	
GPIO27	High : Enable (Internal pull High) VCCACL[1..2], VCCSATAP[1..2], VCCAPLLEXP, VCCFDIPL can remove L/C Low : Disable
Strapping VCC1.5 or VCC1.8	
HDA_SYNC	High : VCC1.5 Low : VCC1.8 (Internal pull Low)



PCH 5/5(POWER)

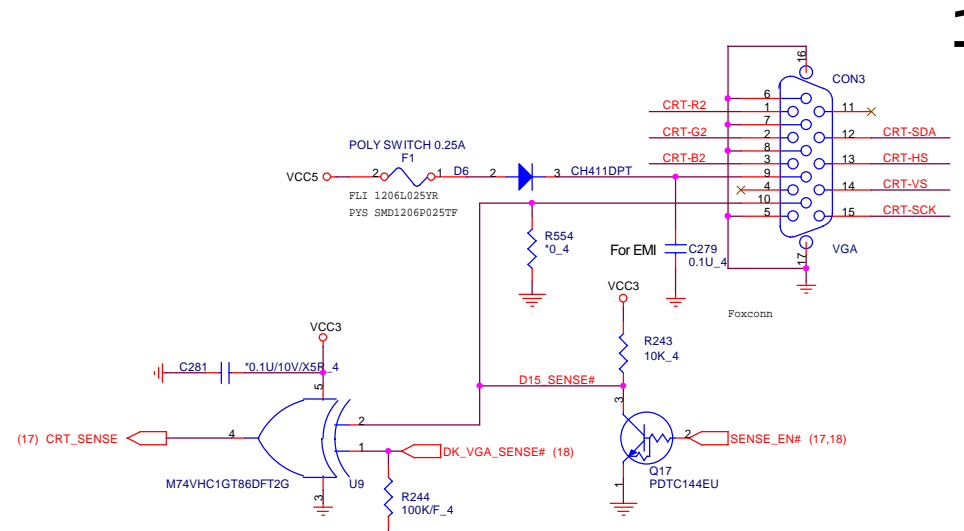
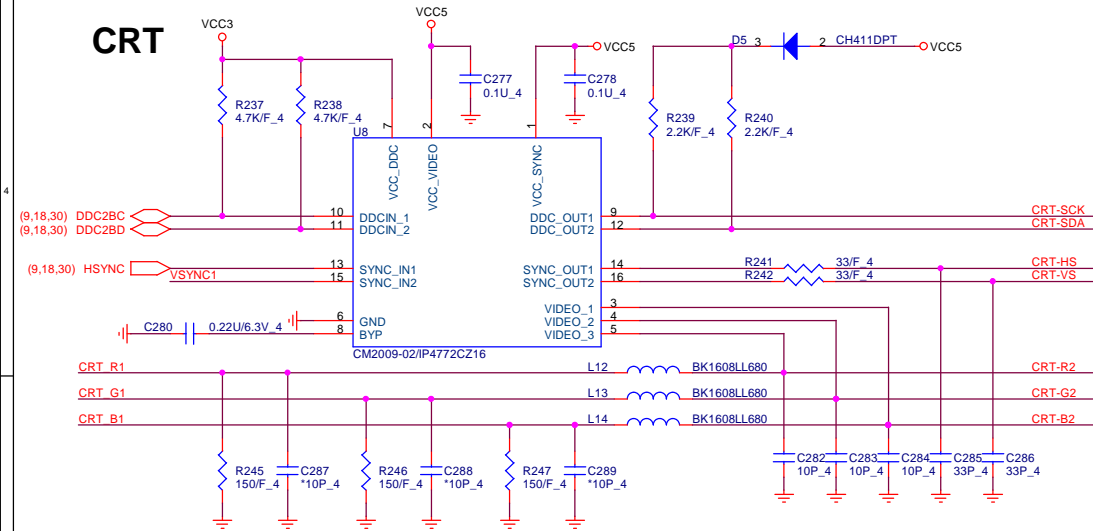
GD3 Main Board

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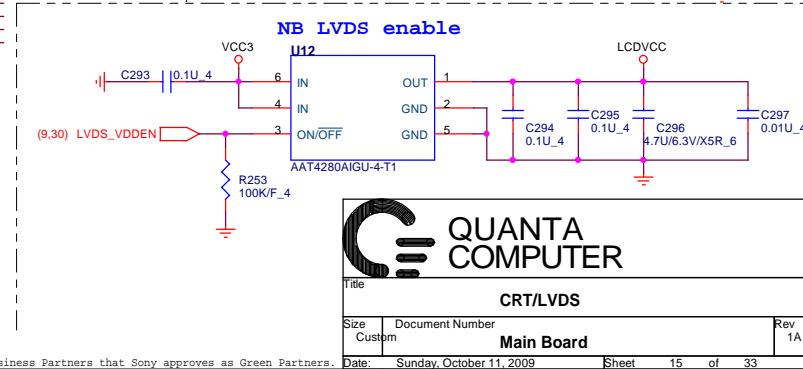
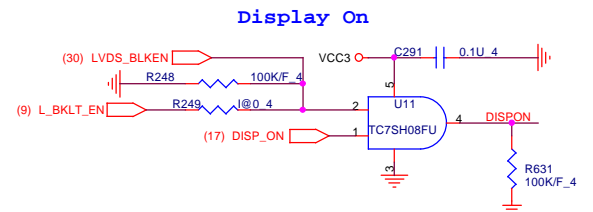
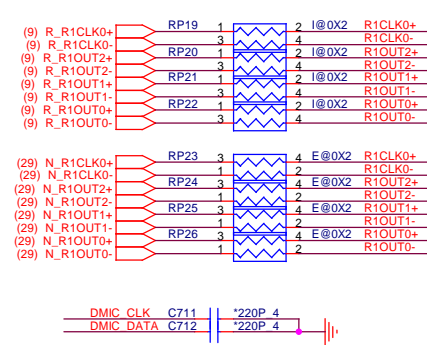
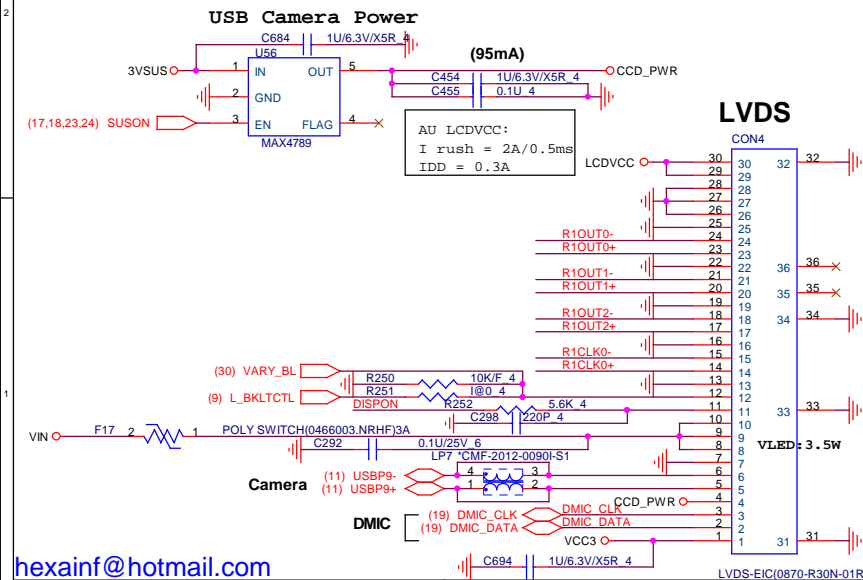
CRT

15

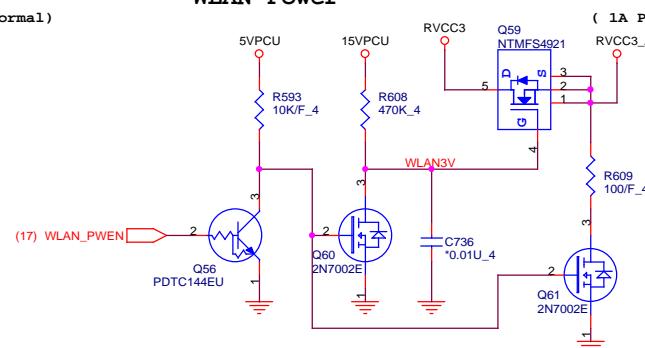


[EC Behavior]
 CRT_SENSE: H=>L or L=>H detect which one is inserting
 Docking_Insert#: H=>L detect which one is inserting
 [CRT SW]
 When Docking_Insert# is low switching RGB to Docking CRT
 [SENSE_EN#]
 Input for CRT pin10, EC assert to high when CRT
 insert[NEO Request]

	SENSE_EN#	DK_VGA_SENSE#	D15_SENSE#	Docking_Insert#	CRT_SENSE
Without Docking					
MB CRT no Plug	L	L	H	H	L
MB CRT Plug in	L	L	H => L	H	L => H
MB CRT plug out	L	L	L => H	H	H => L
With Docking					
All no Plug	L	L	H	L	L
MB CRT Plug in	L	L	H => L	L	L => H
MB CRT plug out	L	L	L => H	L	H => L
DOCK DVI Plug in	L	H => L	H	L	H => L
DOCK DVI Plug out	L	L => H	H	L	L => H
DOCK CRT Plug	L	H => L	H	L	L => L
DOCK CRT/DVI Plug	L	L => H	H	L	L => H

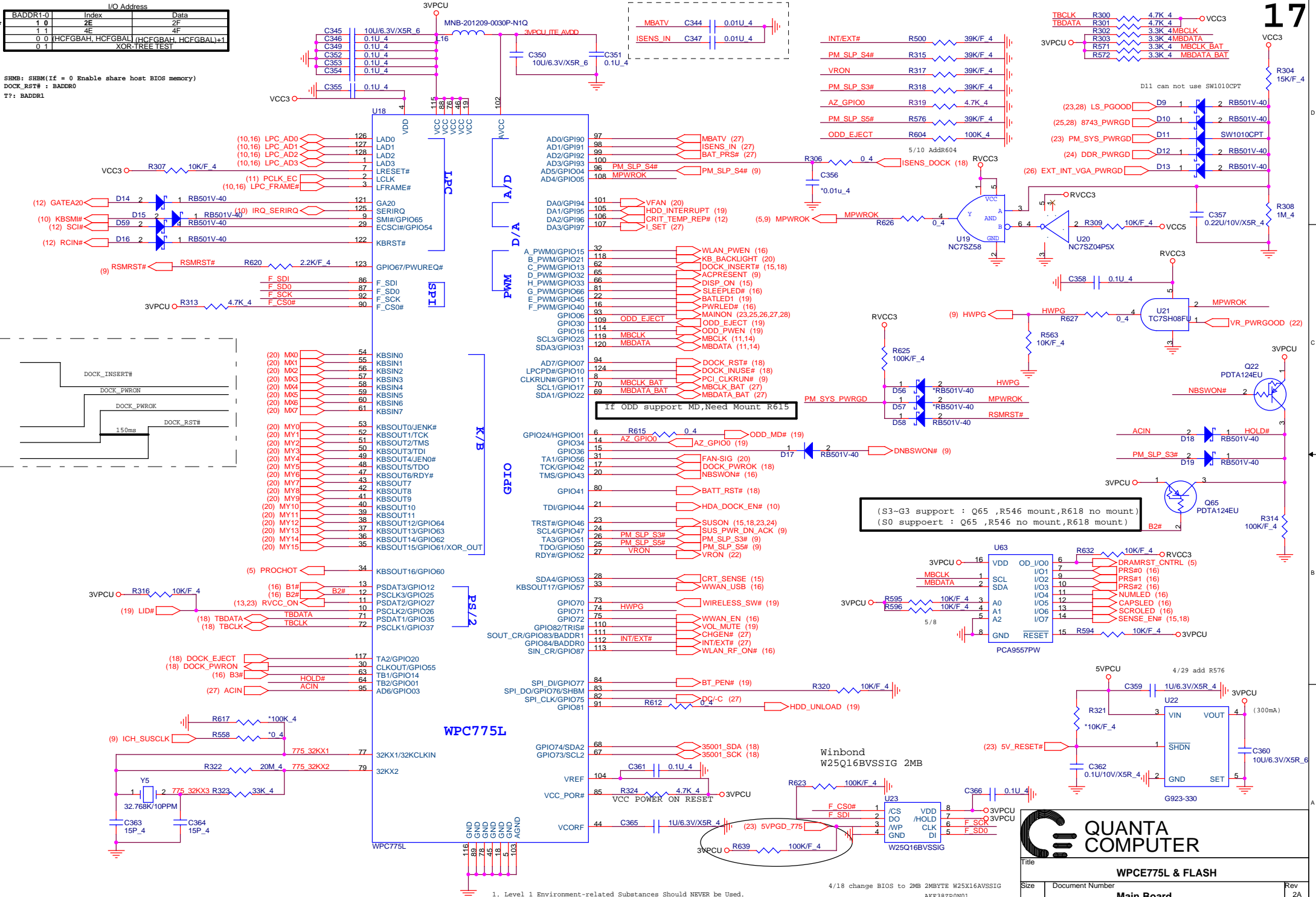



CRT/LVDS			Rev
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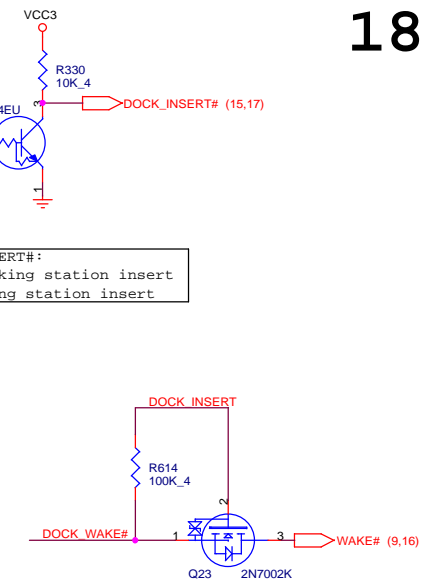
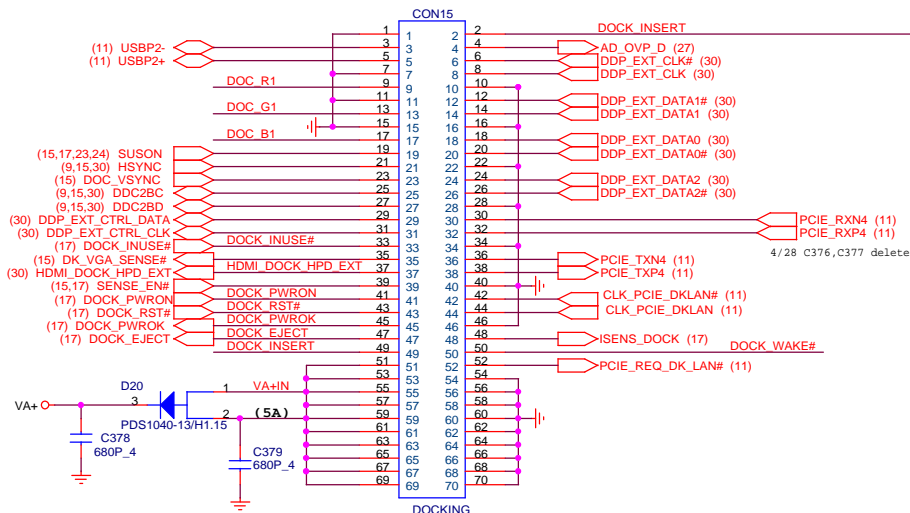
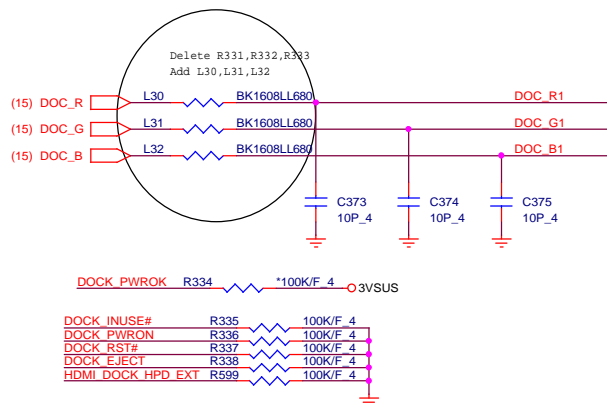
I/O Address		
BADDR1-0	Index	Data
1 0	2E	2F
1 1	4E	4F
0 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
0 1	XOR-Tree Test	

```
SHMB: SHBM(If = 0 Enable share host BIOS memory)
DOCK_RST# : BADDR0
T?: BADDR1
```

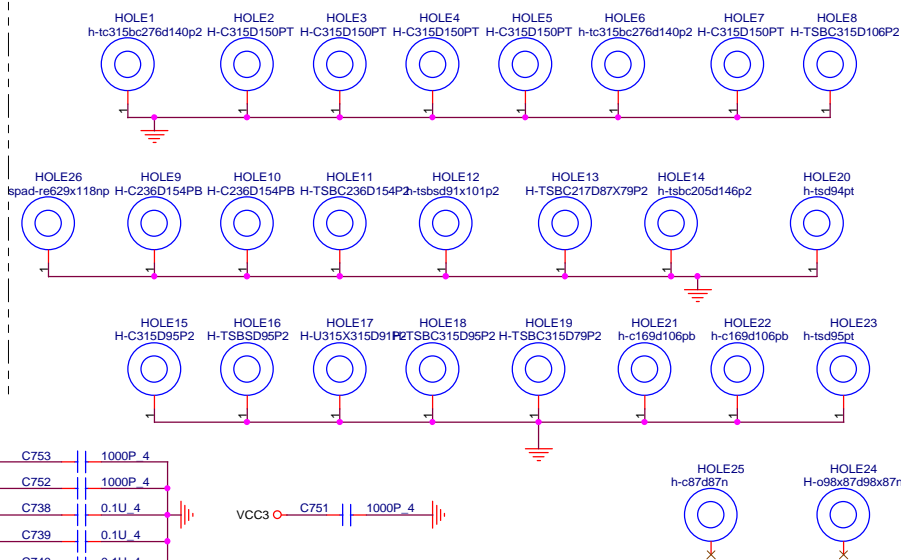
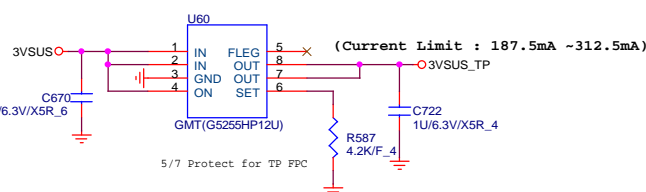
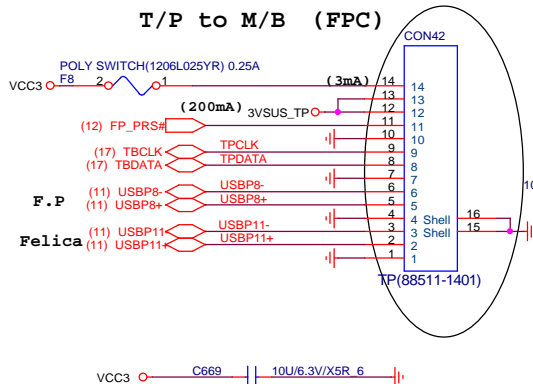


 QUANTA COMPUTER	
Title	
WPCE775L & FLASH	
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	1

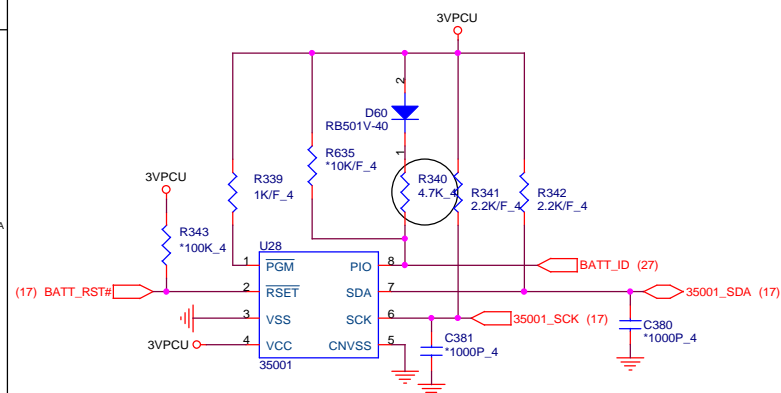
Docking



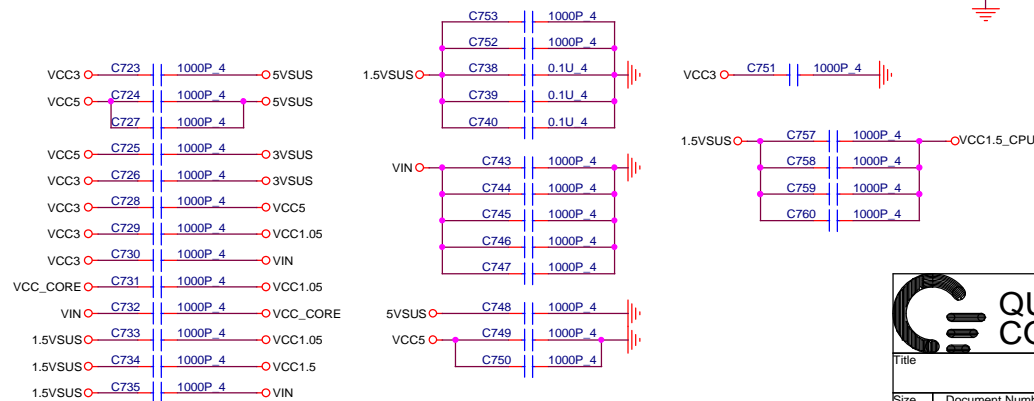
T/P to M/B (FPC)



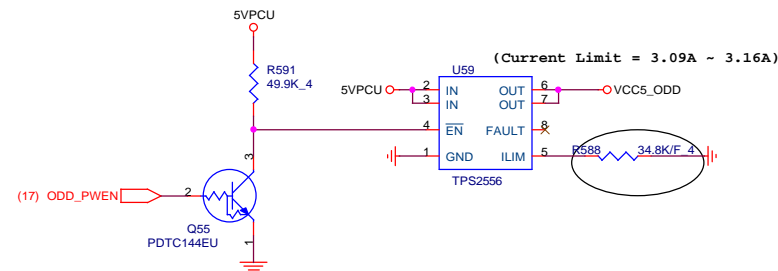
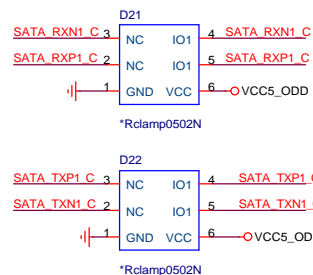
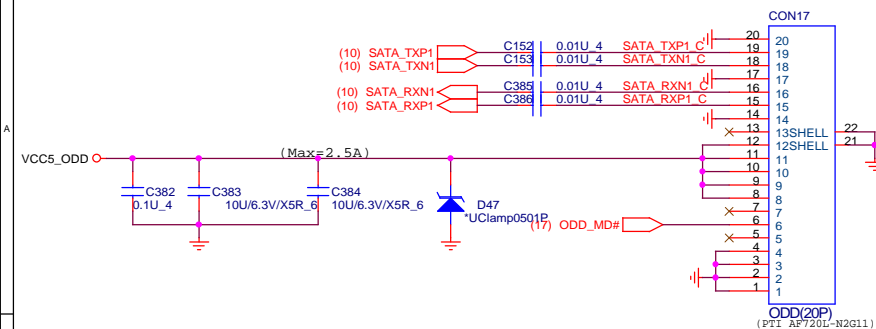
35001



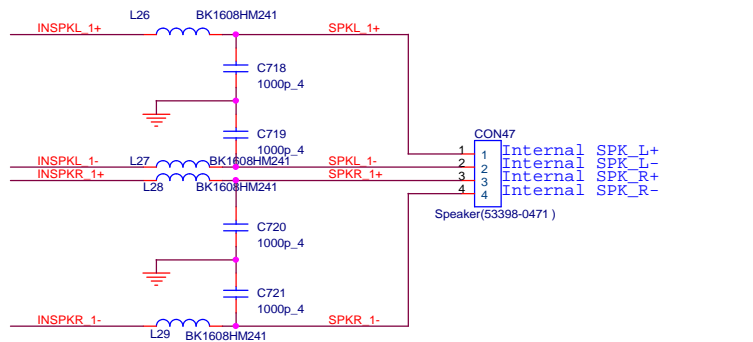
EMI



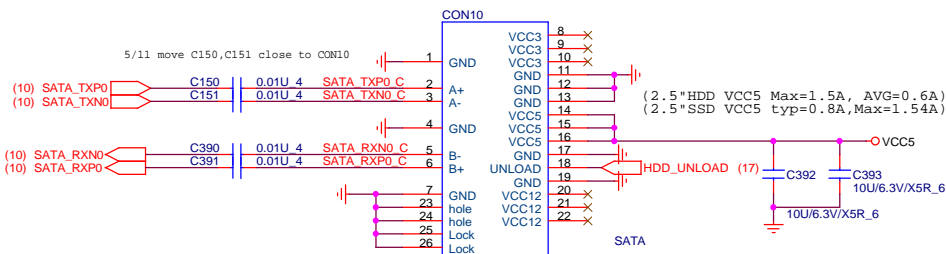
ODD CONNECTOR (FPC 20pin)



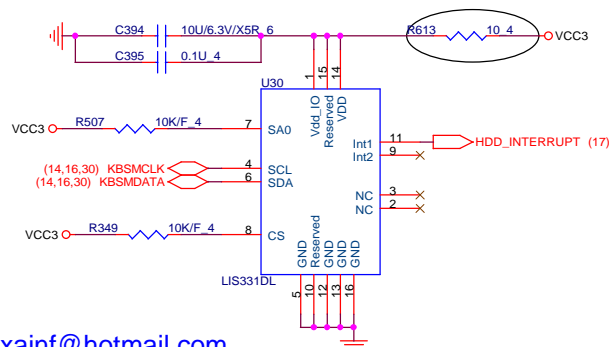
SPEAKER CONNECTOR



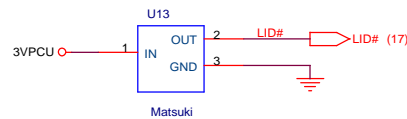
HDD CONNECTOR



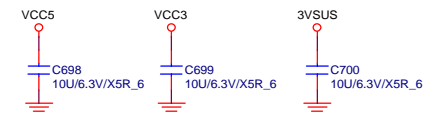
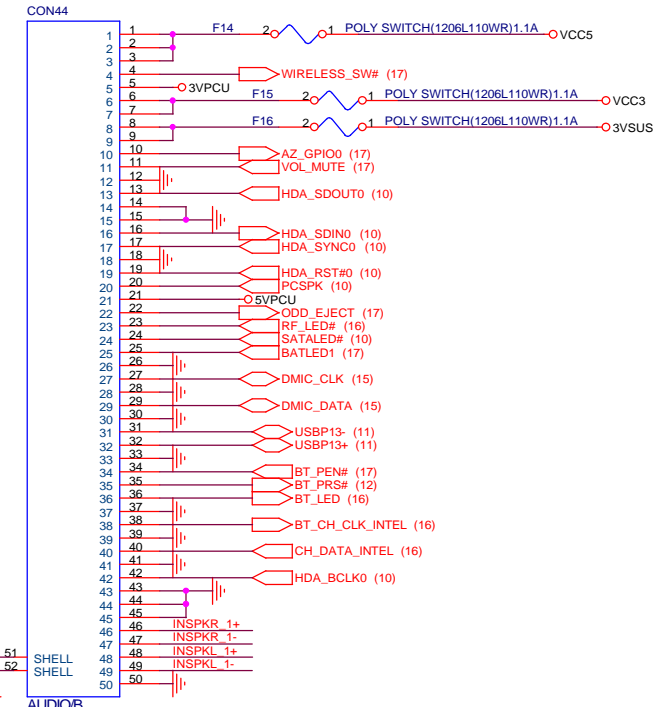
HDD PROTECT



Magnetic Lid Switch



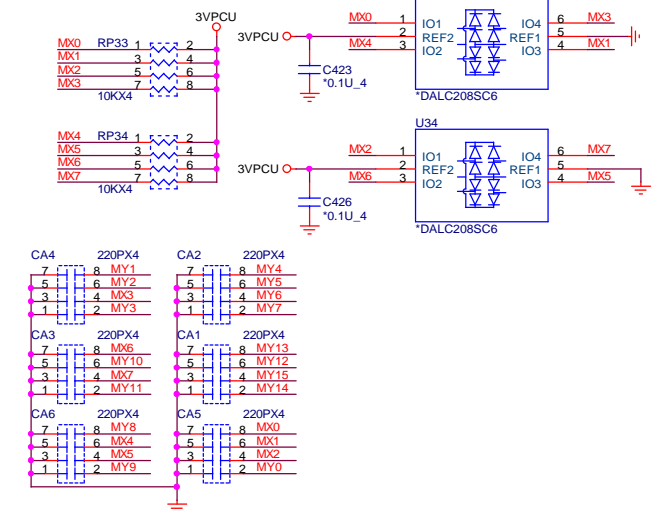
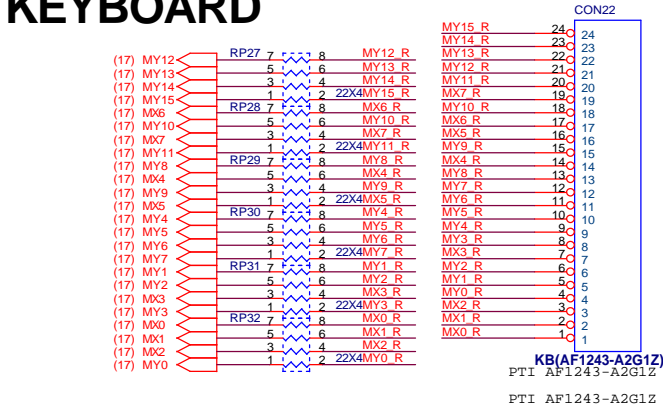
Audio Board



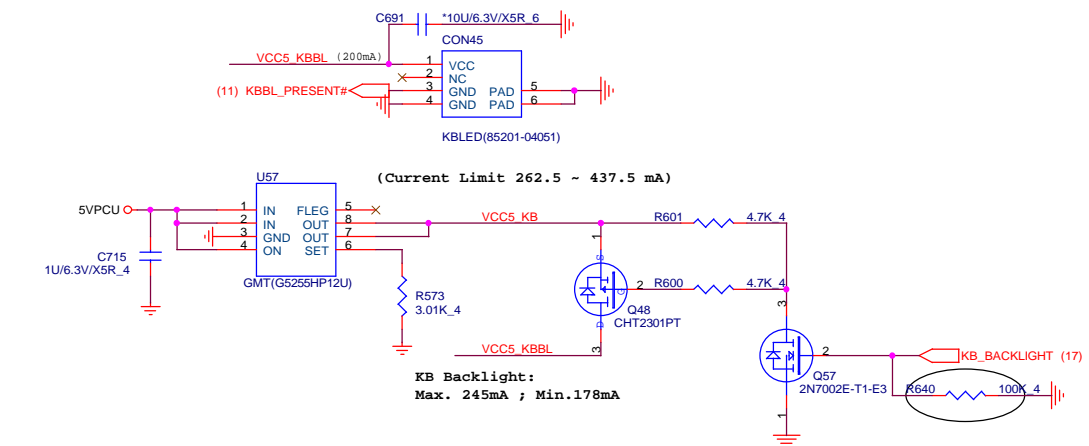
Title		
HDD/ODD/SSD		
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1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the Business Partners that Sony approves as Green Partners.

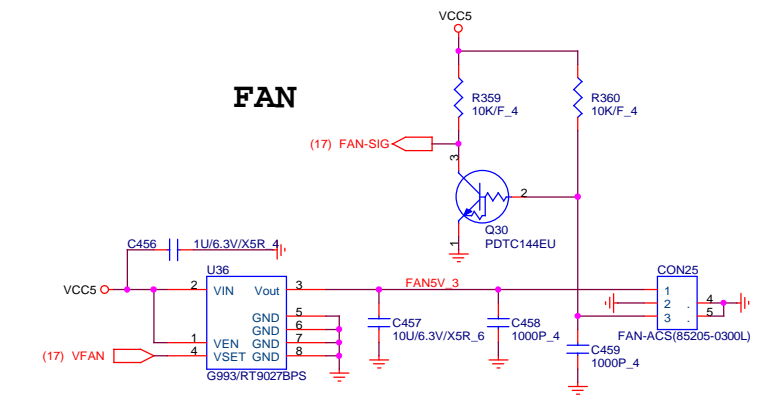
KEYBOARD

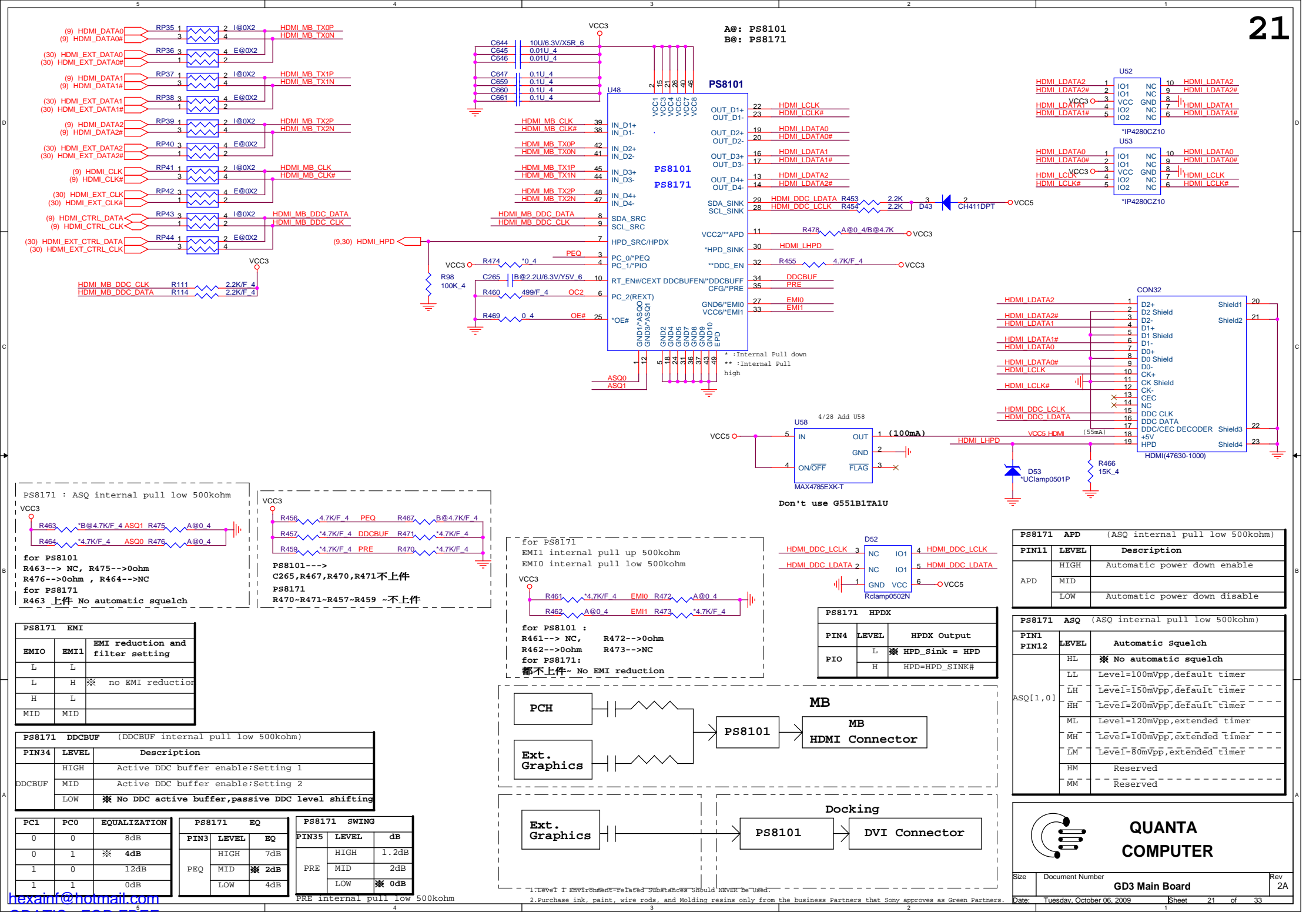


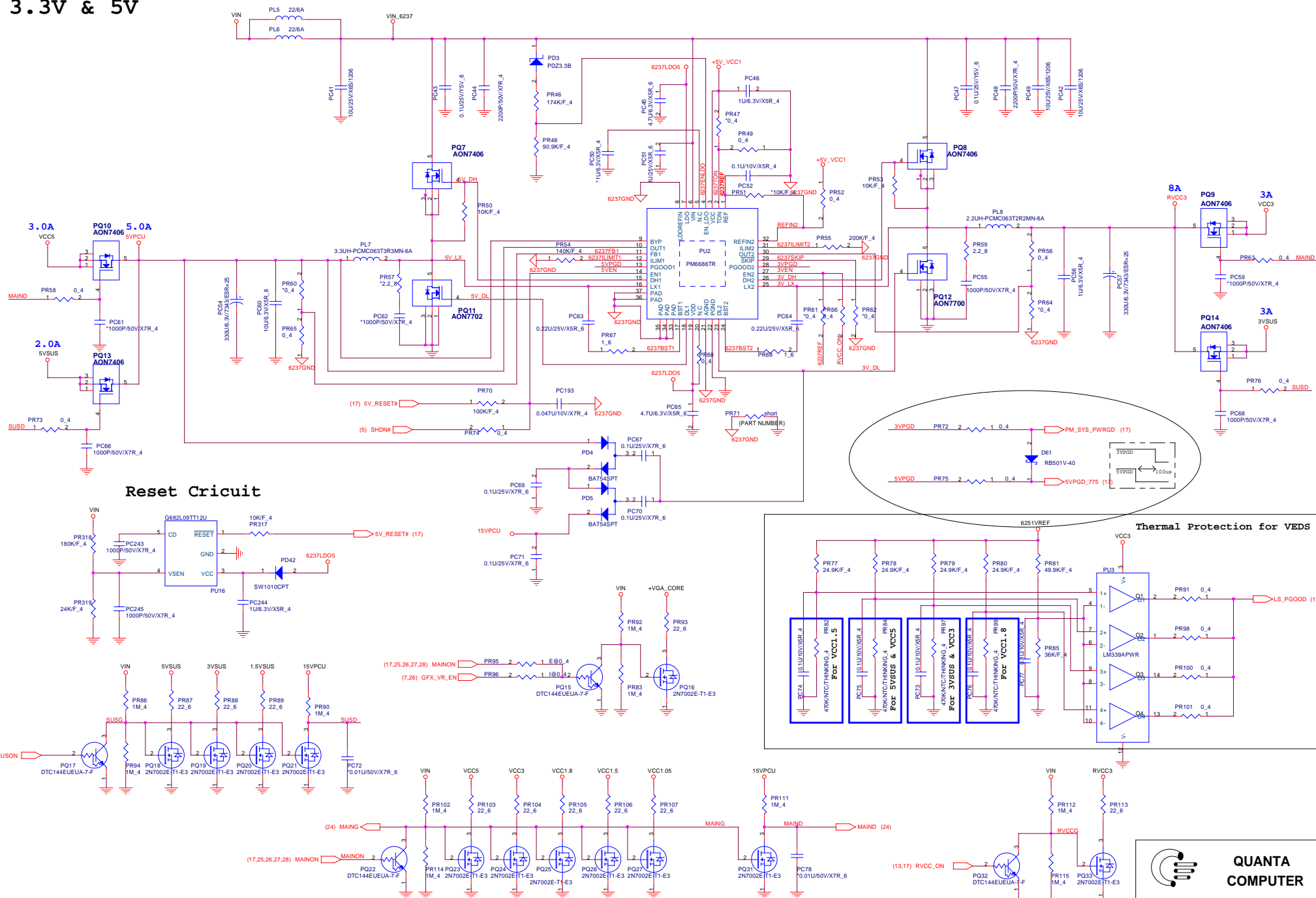
KB BACKLIGHT



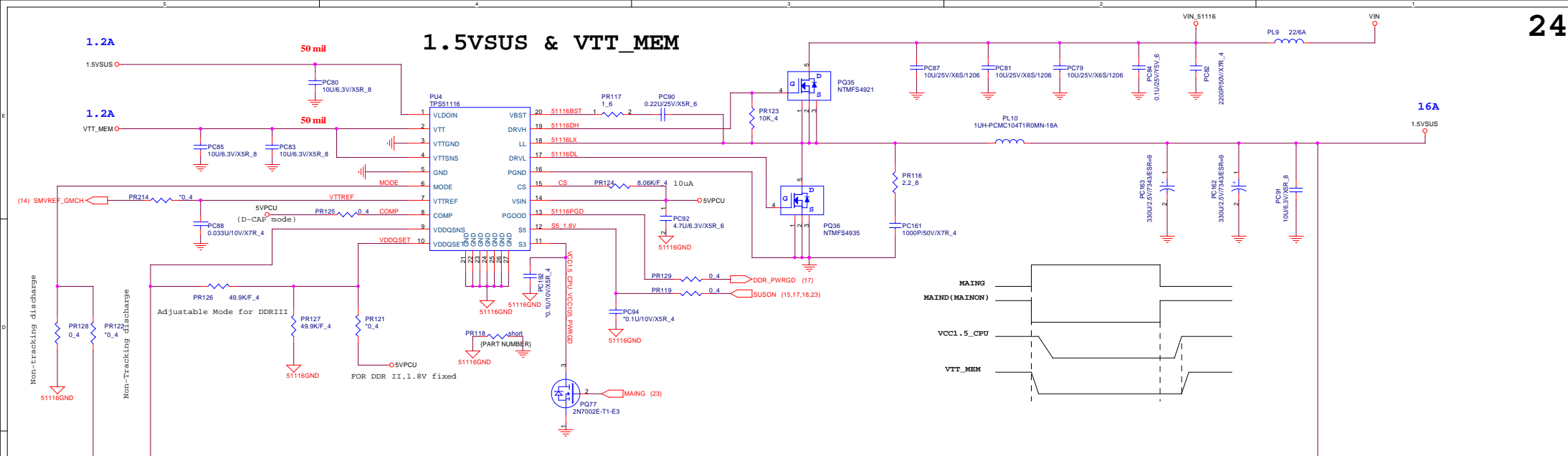
FAN



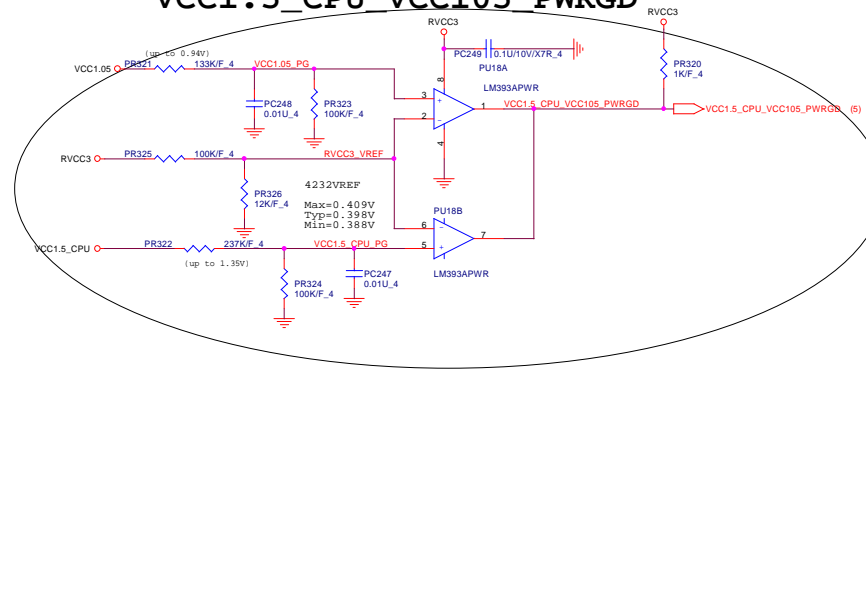




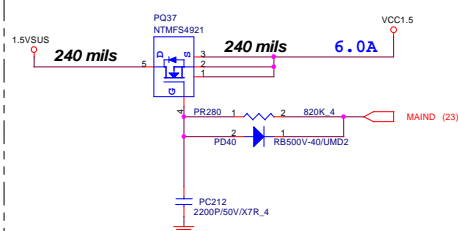
1.5VSUS & VTT MEM



VCC1.5 CPU VCC105 PWRGD

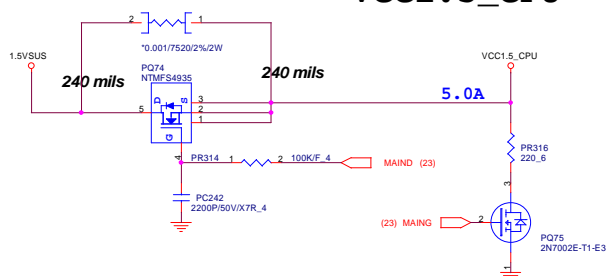


VCC1.5

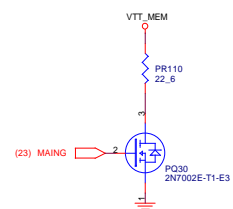


THE CIRCUIT NOT CHECK P/N

VCC1.5 CPU



VTT_MEM Discharge



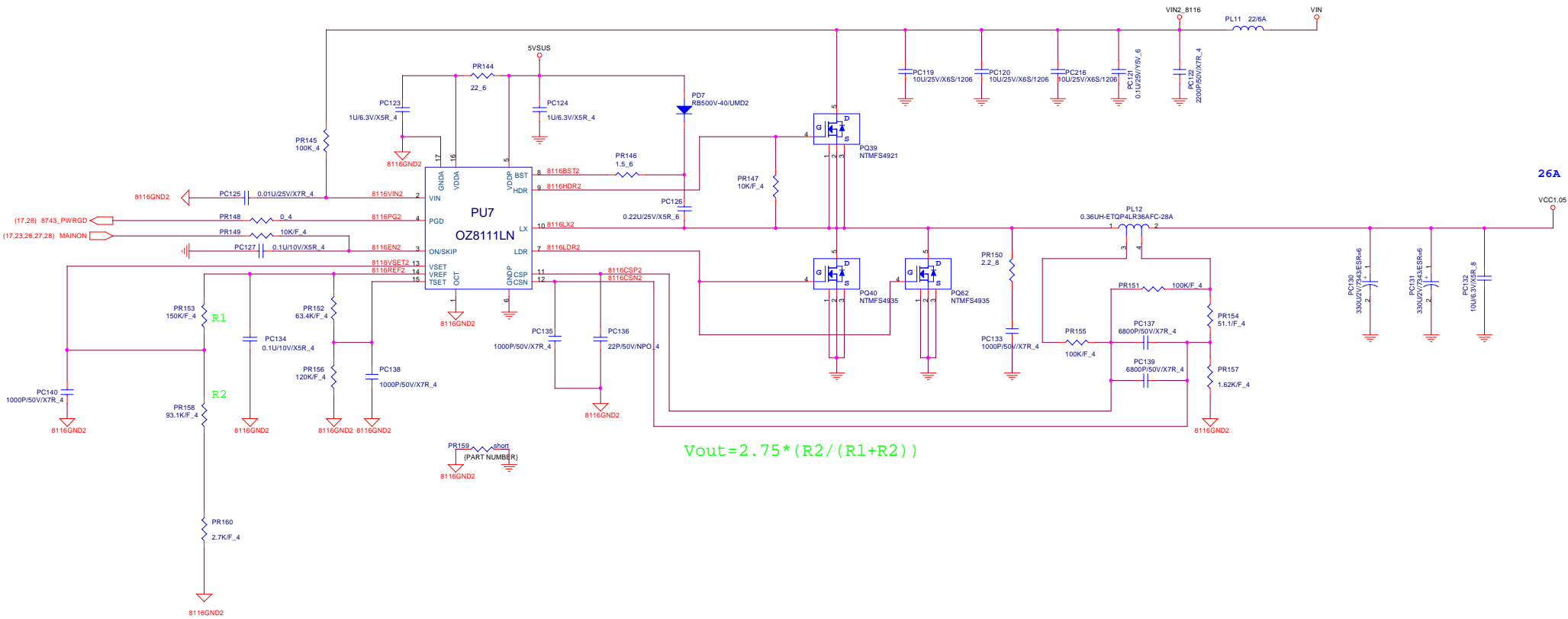
MODE	DISCHARGE MODE
+5V	No discharge
+1.8V	Tracking discharge
GND	Non-tracking discharge

VDDQSET	VDDQ(V)	VTTREF & VTT	NOTE
GND	2.5 fixed	VDDQSNS/2	DDR
5V	1.8 fixed	VDDQSNS/2	DDR2
FB-Resistor	Adjustable	VDDQSNS/2	1.5V<VDDQ<3V

$$V_{TT} = V_{TTREF} = V_{DDQSNS}/2 = 0.9V$$


STATE	S3	S5	1.8VSUS	VTTREF	VTT
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off





(Ext. Graphice Plaes NDI
PQ41,PR161)

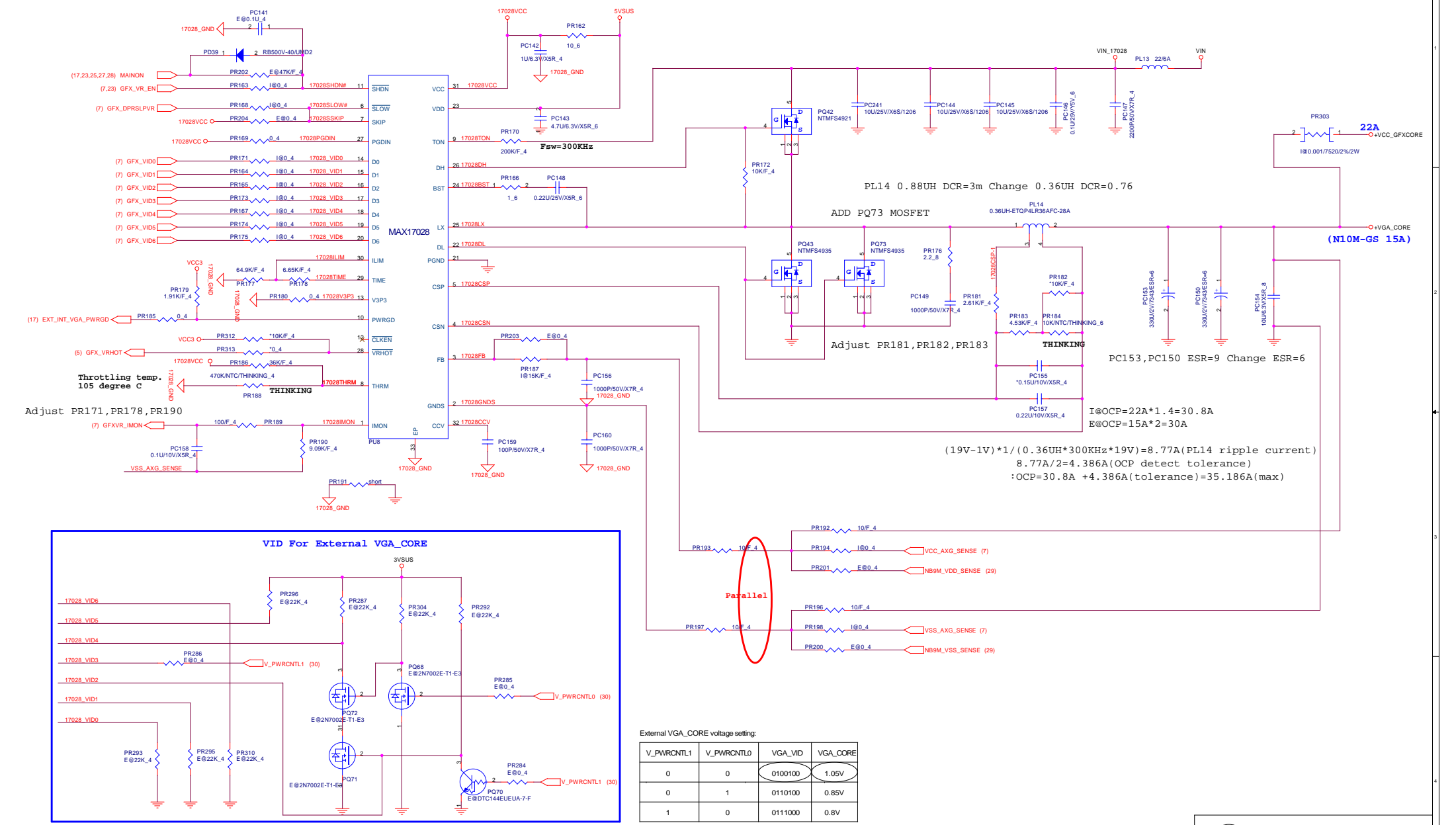
VTT_SEL	VCC1.05-1
High	1.05V
Low	1.10V

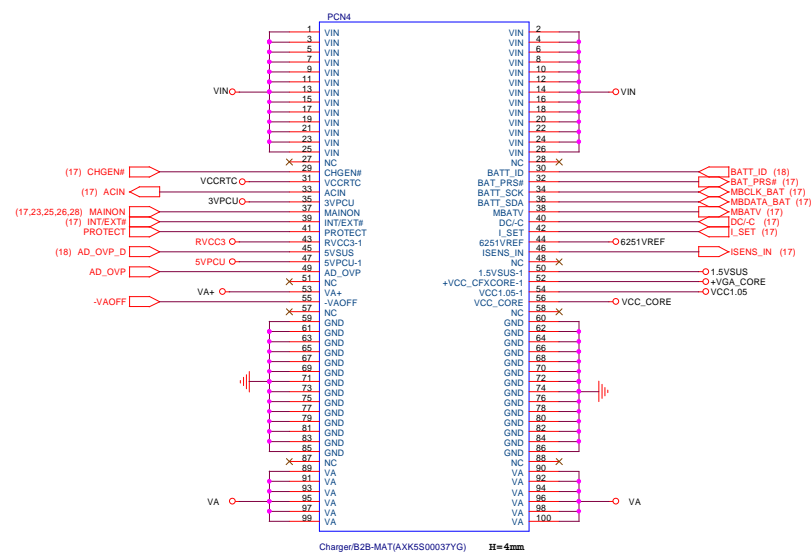
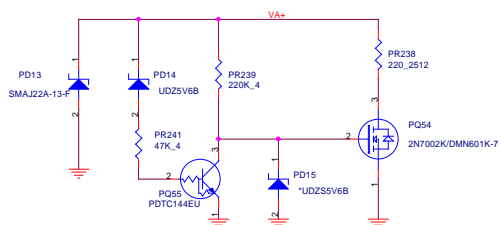
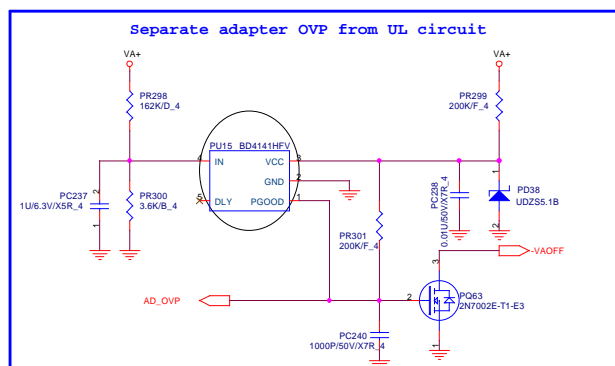
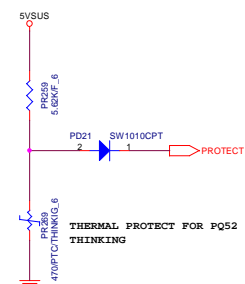
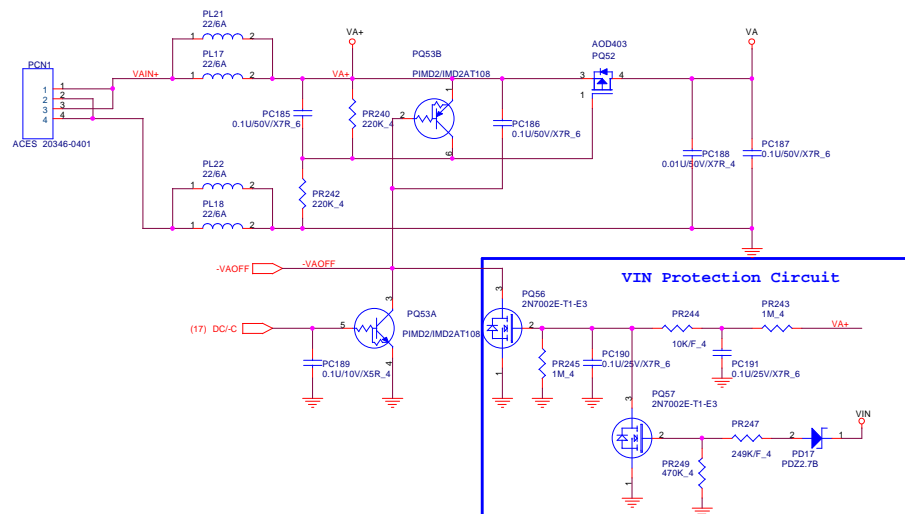


**QUANTA
COMPUTER**

Size	Document Number	Rev
	GD3 Main Board	1A
Date:	Monday, October 05, 2009	Sheet 25 of 33

1.Level 1 Environment-related Substances should NEVER be Used.
2.Purchase ink, paint, wire rode, and Molding resins only from the business Partners that Sony approves as Green Partners.





**QUANTA
COMPUTER**

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	GD3 MB	1A
Date:	Tuesday, October 06, 2009	Sheet 27 of 33

1. Level 1 Environment-related Substances should NEVER be used.
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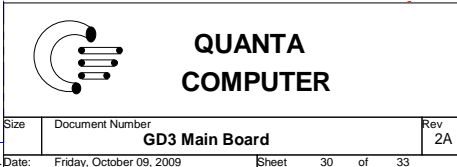


V_PWRCNTL1	V_PWRCNTL0	VGA_VID	VGA_CORE
0	0	0101000	1.0V
0	1	0110100	0.85V
1	0	0111000	0.8V

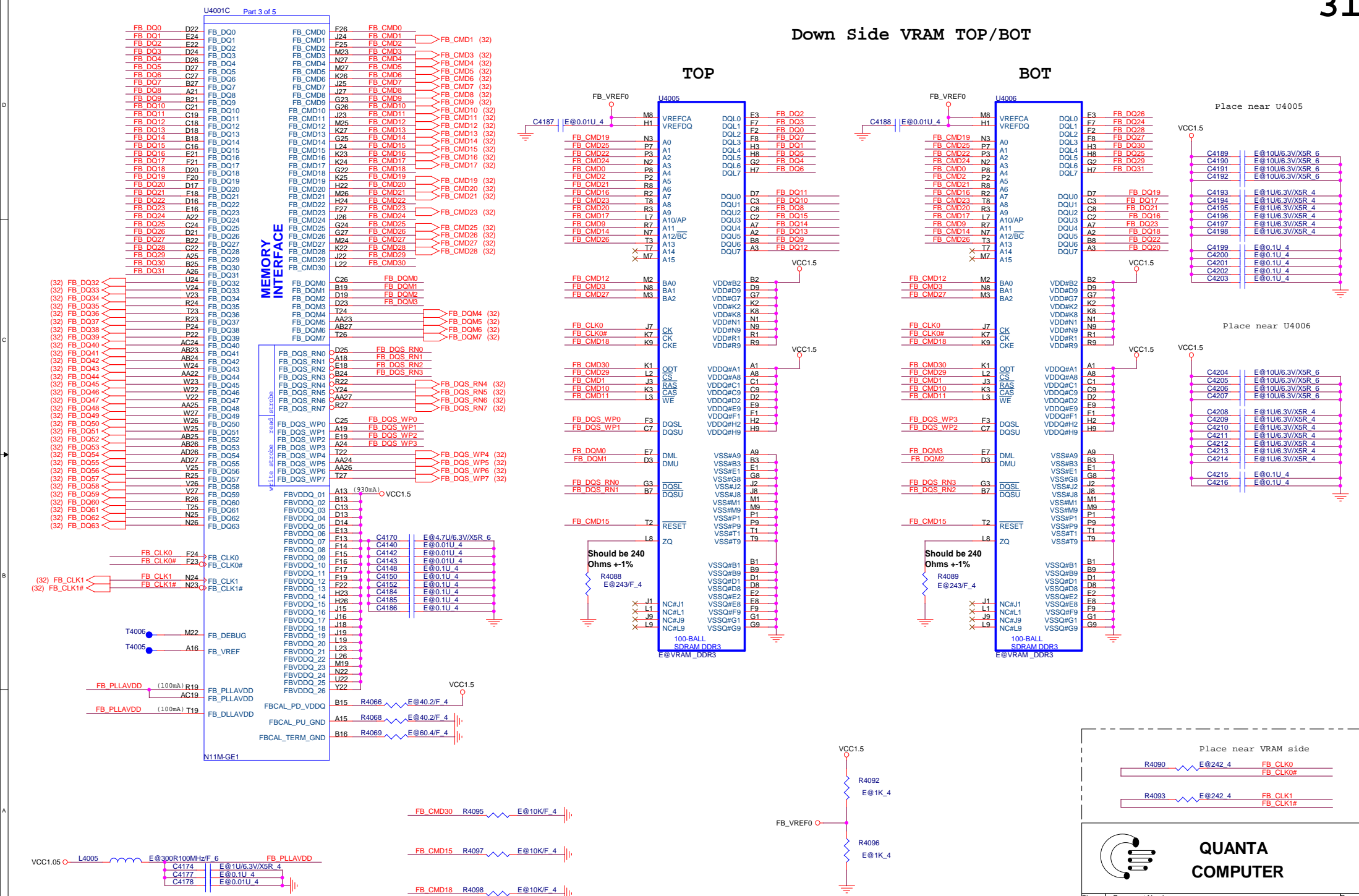
Resister Value	Pull to VDD	Pull to GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Straps	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG [3]	3GIO_PADCFG [2]	3GIO_PADCFG [1]	3GIO_PADCFG [0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]

VRAM Capacity	VRAM Vender	ID	R4028
DDR3 64Mx16	Samsung	0011	PD20K
	Hynix	0010	PD15K

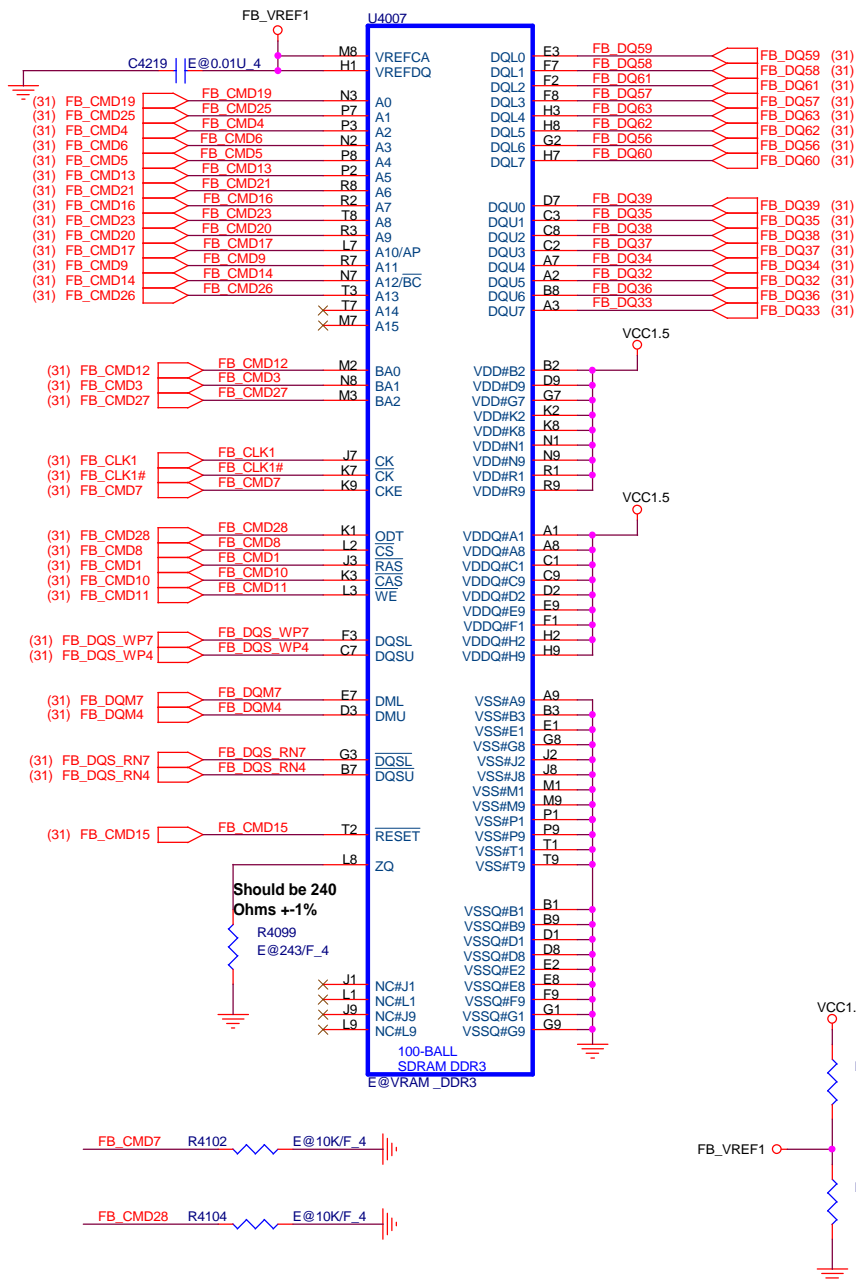


Down Side VRAM TOP/BOT

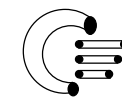
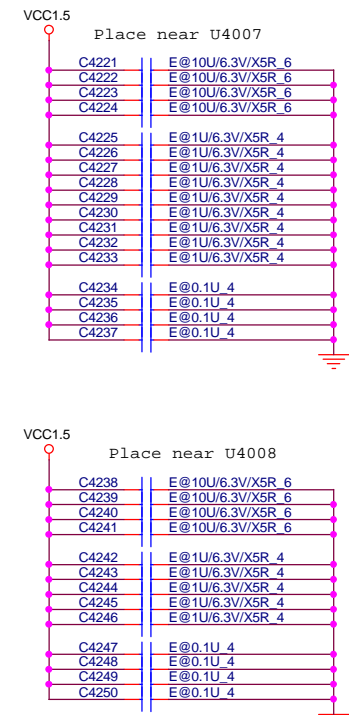
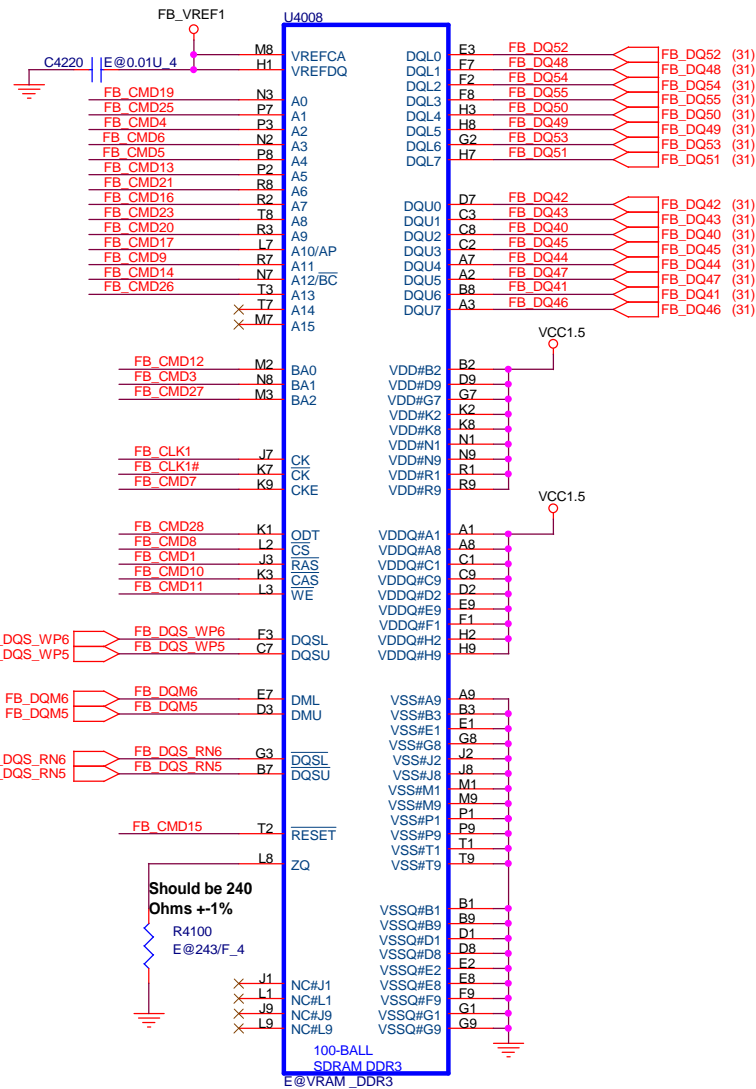


Up Side VRAM TOP/BOT

TOP



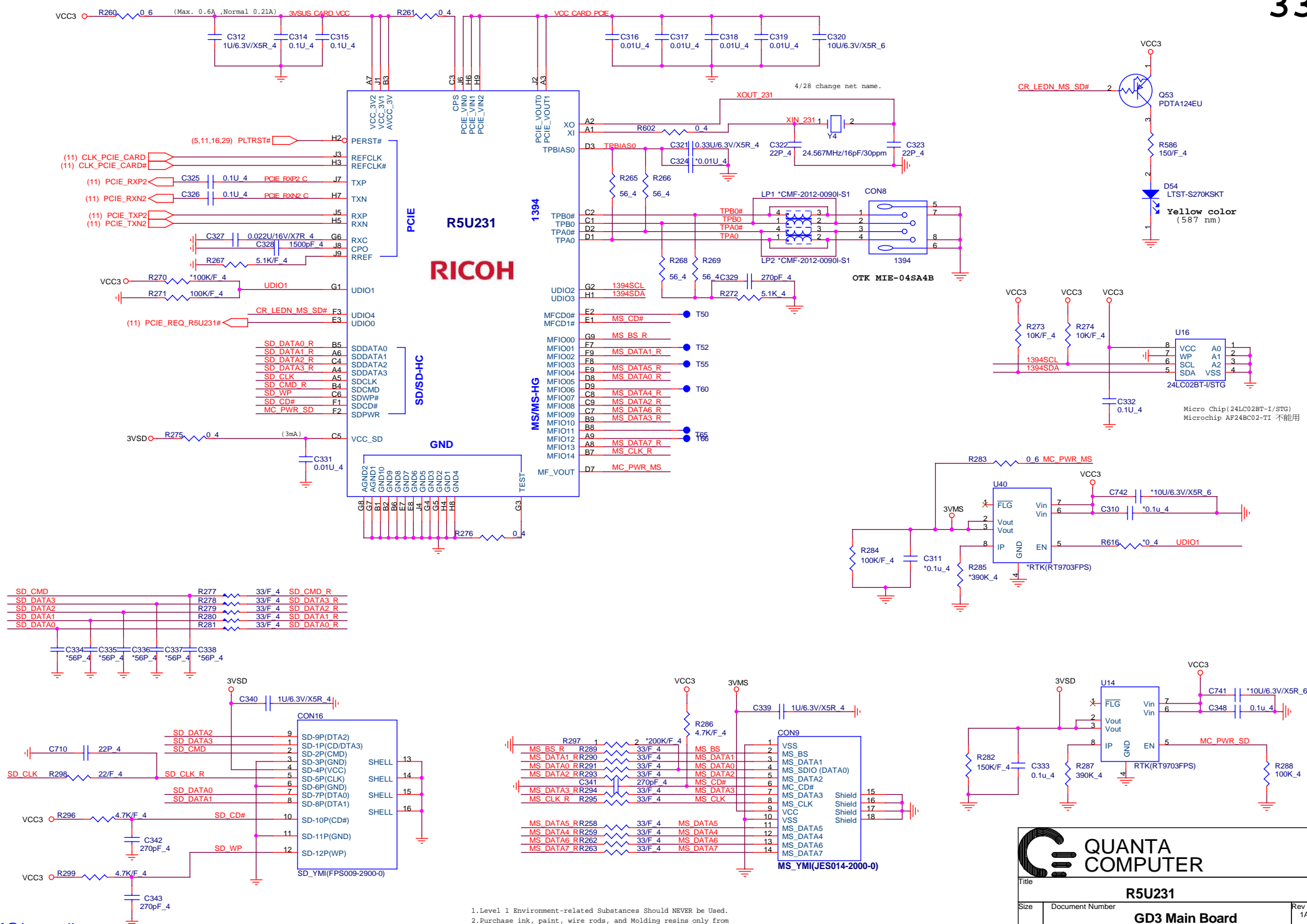
BOT



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Size	Document Number	Rev
	GD3 Main Board	1A
Date:	Monday, October 05, 2009	Sheet 32 of 33



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Title			R5U231		
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GD3 Main Board					
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